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	D. F. Kostishack
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LEXINGTON, MASSACHUSETTS

This technical report has been reviewed and is approved for publication.

FOR THE COMMANDER

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MASSACHUSETTS INSTITUTE OF TECHNOLOGY

LINCOLN LABORATORY

.

EBS (ELECTRON BOMBARDED SEMICONDUCTOR) RF AMPLIFIER DESIGN

D. F. KOSTISHACK*

Division 3

TECHNICAL NOTE 1975-44

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LEXINGTON   MASSACHUSETTS

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ABSTRACT

This report presents a comprehensive design criteria for EBS RF power amplifiers which incorporates all pertinent design parameters associated with both the electron beam and semiconductor diode targets. The derivation of the design model is described in detail, and an example amplifier design is carried out yielding an optimum set of device specifications and summary of predicted performance.

TABLE OF CONTENTS

1.0 INTRODUCTION

During the past several years a new device concept which involves both semi-
conductor and vacuum tube technologies has received increasing interest for application
to microwave power amplifiers. The Electron Bombarded Semiconductor (EBS)
Amplifier promises many advantages over state-of-the-art transistors and tubes
with respect to output power capability, efficiency, gain, circuit simplicity, size
and weight, bandwidth, cutoff frequency, and linearity.[1,2] Until recently a con-
siderable amount of research has been directed toward solving the many non-trivial
problems associated with mating these two technology areas. The device, which
incorporates a state-of-the-art electron gun and large area shallow junction semi-
conductor diode targets, has been developed to a level such that optimization of
performance has become an important consideration.

Several device models have evolved which for the most part deal with a purely
theoretical analysis or consider only a few of the numerous technological requirements
and limitations. This report presents a comprehensive design criteria for EBS RF
power amplifiers which incorporate all of the pertinent design parameters associated
with both the electron beam and diode targets. The analysis includes in addition to
the basic static diode carrier transport relationships:

    a)   dynamic analysis based on realistic current or voltage complex
            waveforms,

    b)   realizable output circuit parameters for finite bandwidth,

    c)   diode power dissipation restrictions based on actual thermal impedances
            associated with the geometric shapes and types of materials used,

    d)   avalanche breakdown voltage analysis for actual diode junction
            geometries and impurity profiles, and

    e)   optimization of design for a specific performance requirement which
            includes the overall amplifier efficiency (including beam power) in
            addition to the diode collector efficiency.

The design model is basic enough to accommodate different semiconductor materials, e-beam structures, frequency of operation, and output power and gain requirements. It is sufficiently detailed and complete to provide exact design specifications, such as geometries for the e-beam and diode, and circuit network values to be applied directly to the fabrication of practical amplifiers. Although the established design criteria are primarily applied to high average power amplifiers at microwave frequencies, the analysis can be used in designs for other applications such as pulsed low duty factor amplifiers, and high current or voltage pulse video amplifiers.

A portion of the design analysis, specifically the dynamic waveform analysis, was derived by R. B. Adler and W. Gross of the Electrical Engineering Department of the Massachusetts Institute of Technology through a consulting contract as part of the Lincoln Laboratory EBS Program. The results of their study are reported in Ref. 3 and extended here to the total amplifier design criteria presented below.

The EBS device concept is based on the physical mechanism that a stream of high energy electrons penetrating a semiconductor material ionize electron-hole pairs which become current carriers when an electric field is present in the semiconductor. The EBS device is essentially a miniature vacuum tube structure. As shown in Fig. 1, an electron gun is used to generate a moderate current beam of several mA focused to a specific diameter. The target or anode is a relatively large area, shallow junction semiconductor diode which is reverse biased below breakdown voltage with the output load impedance connected across the diode. The small input RF signal causes the e-beam to be density modulated (with a grid or helical traveling wave structure) or position modulated using deflection plates or a meander shaped transmission line. These techniques modulate the current of the beam which impinges on the active diode area. Approximately one electron-hole pair is generated for every 3. 6 electron volts of energy for each beam electron for a target of silicon. Consequently, a 3 mA, 10 kV electron beam can induce 6 A of useful
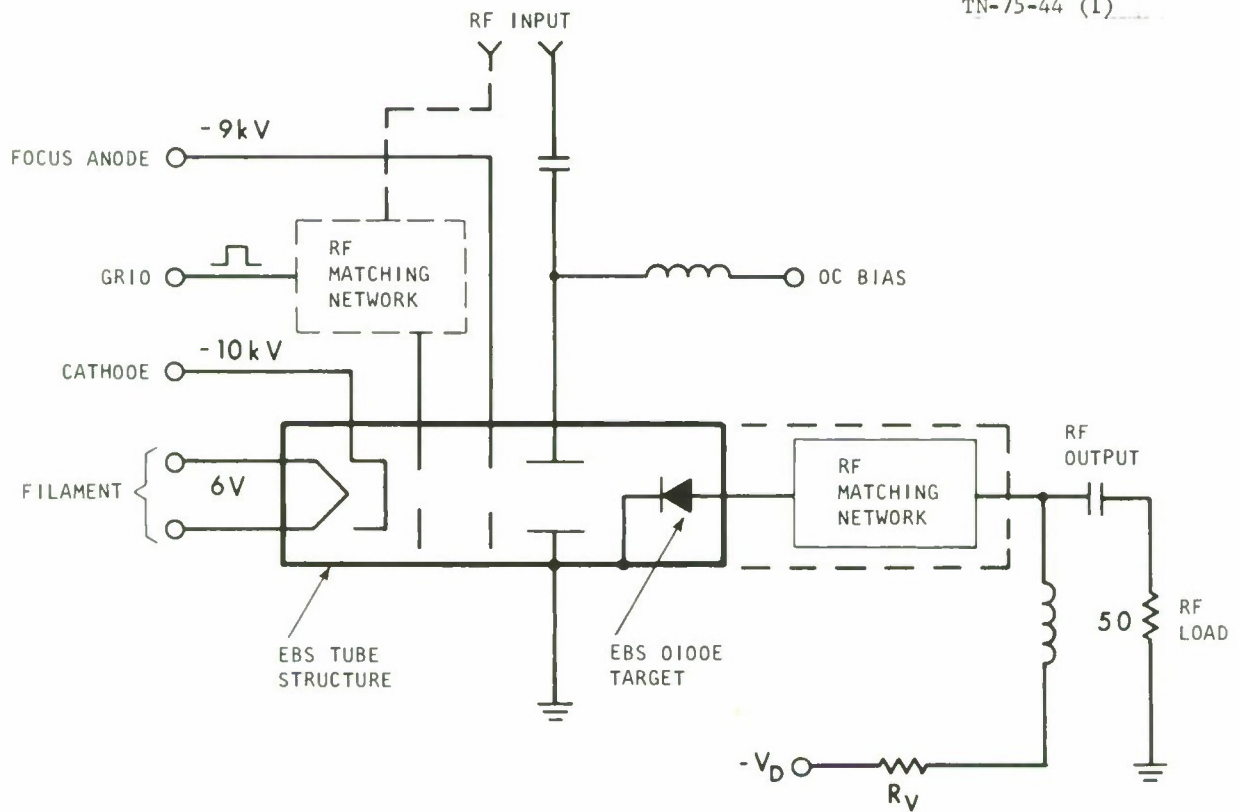
2

Fig. 1. Schematic of EBS RF amplifier.

current in a low surface loss diode target. Figure 2 presents typical current gain characteristic curves for a p+n silicon diode target. The application of this high current gain mechanism to a useful RF amplifier is developed in the following analysis.

2.0 Device Analysis

The following analysis of the EBS amplifier will employ a simple but reasonably complete model of the electron beam and semiconductor diode target structures. The geometry of the shallow junction large area diode is shown in Fig. 3. An abrupt junction p+nn+ doping density profile is assumed for the diode with a circular planar geometry. A relatively deep diffused guard ring is used to reduce the high electric field effects at the edge of the shallow diffused p+n junction which would otherwise result in drastically reduced breakdown voltages. A n-type base region diode is selected versus a p-type simply because the higher scattering limited velocity of electrons compared to holes permits efficient operation at higher frequencies. The nn+ base region of the diode is epitaxially grown to ensure a relatively abrupt transition in doping density; a requirement for sustaining the high electric field punch-through condition of the depletion region of the reversed biased diode.

The electron beam used in this model is a thin cylindrical or pencil beam which is either density modulated or deflected on and off the target diode active area by the RF input power to the tube structure.

2.1 Diode Current, Voltage, and Output Power

The current (electrons) inside the reverse biased diode induced by the high energy electron beam is assumed to be uniformly distributed across the diode active area and perpendicular to the exposed surface of the shallow junction. With no beam impinging on the diode, the current density is zero since the reverse saturation current is insignificantly small. It reaches a peak value (J_{pk}) determined
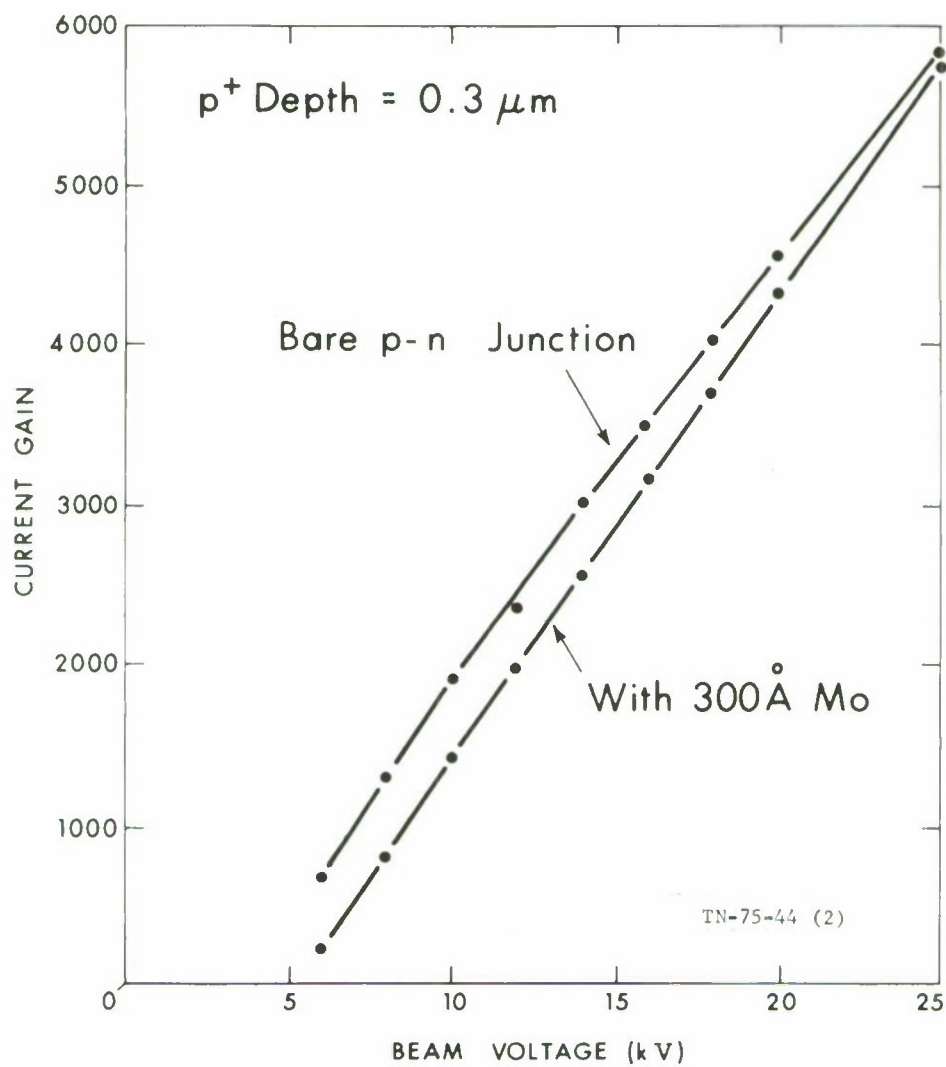
Fig. 2.   EBS diode current gain.

GOLD FOIL SHIELD

GOLD

MOLYBDENUM

THERMAL SiO_2

n^+- CHANNEL STOP

p^+-GUARD RING
(OPTIONAL)

SHALLOW p^+-DIFFUSION

n- EPITAXIAL LAYER
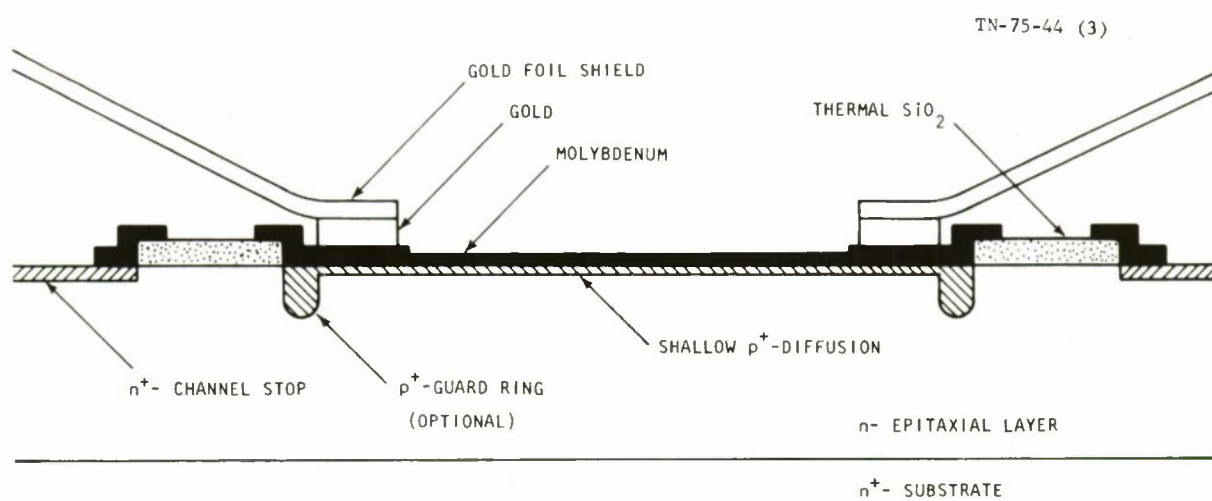
n^+- SUBSTRATE

Fig. 3.   Silicon EBS diode geometry.

6

by the peak beam current density on the diode and results typically in a non-sinusoidal current waveform.   For high frequency operation it is desirable to maintain the scattering limited velocity for the electrons which reduces the transit time of the electrons through the base region of the diode to a minimum.   Thus, it is necessary to maintain an electric field at any point in the diode at values greater than the minimum value E_{sat} required for velocity saturation.   This can be accomplished if the voltage across the device during the RF voltage swing does not fall below a minimum value:

$$V_{min} = W E_{sat} \tag{1}$$

where W is the width of the depletion region of the reverse biased p+n junction. For the present case in which this region reaches the nn+ interface with the punch-through condition, W is also the physical length of the n-type base region of the p+nn+ structure.   In addition, the space charge density due to the current carrying electrons must not exceed the background donor density of the n-type region N_D, such that,

$$J_{pk} = q\, v_{scl} N_D \tag{2}$$

where q = charge of an electron and v_{scl} = scattering limited velocity.

For values of current density greater than J_{pk}, the electric field would be depressed below the E_{min} value since the voltage across the diode has reached V_{min} simultaneous with J equal to J_{pk} during the cycle.   The maximum voltage during a RF cycle across the diode is limited by the requirement that the device not go into avalanche breakdown which would lead to a low efficiency operation if not a catastrophic failure.   The breakdown condition is initiated if the field at any point in the diode exceeds a maximum value, E_{max}, which, in general, is a function of the doping density and temperature.   Figure 4 is an experimentally determined curve of E_{max} versus doping density at a temperature of 300° K. E_{max} increases slightly
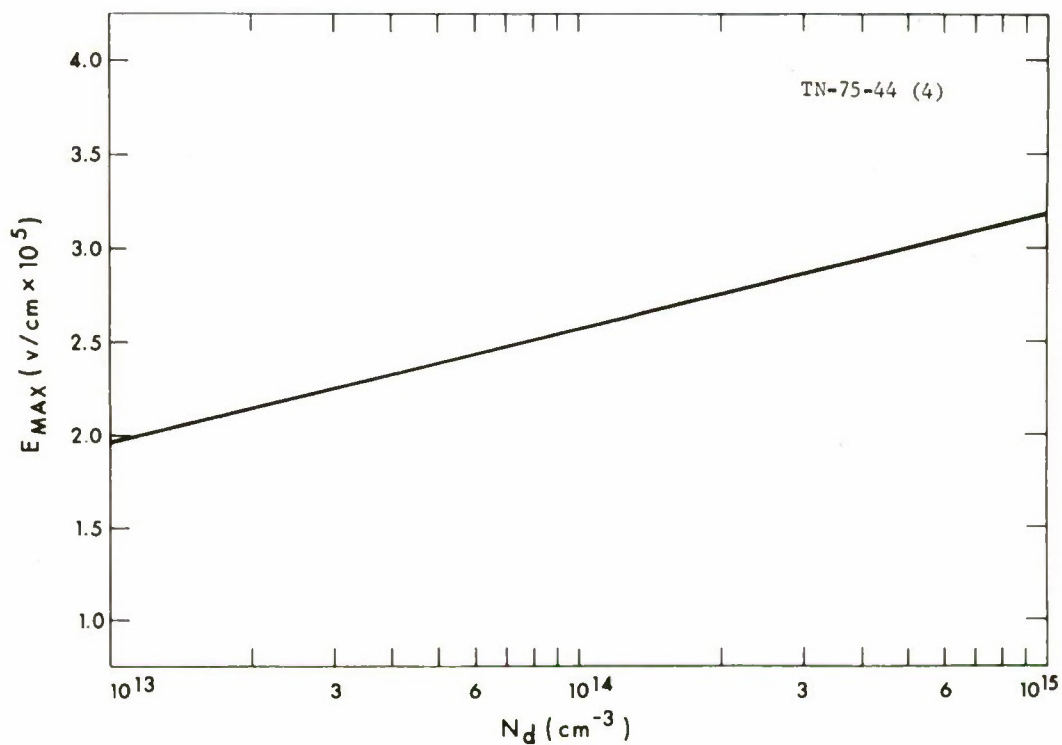
7

Fig. 4. Maximum electric field allowed in silicon, E_{max}, at 300°K versus impurity concentration, N_d.

(G. Gibbons and S. M. Sze, "Breakdown Fields in Silicon," Solid-state Electronics 11, pp. 275 - 232 [February 1968])

for higher temperatures. The electric field profile for the assumed p^+nn^+ diode structure is shown in Fig. 5 for a bias voltage slightly less than breakdown voltage. From Poisson's equation,

$$\frac{\partial^2 V}{\partial X^2} = \frac{-\rho}{\epsilon}, \tag{3}$$

where ρ = net charge density and ϵ = dielectric permittivity, the voltage across the device is related to the field by

$$V = -\int_O^{W'} E(X)\, dX. \tag{4}$$

Solving this for the given profile of Fig. 5, the breakdown voltage is

$$V_{BD} = W' \left[E_{max} - \frac{1}{2} \frac{qN_D}{\epsilon\, \epsilon_o} W' \right]. \tag{5}$$

For the present model, the guard ring structure is more deeply diffused than the shallow active area junction and, therefore, the fields should reach E_{max} between the guard ring and nn+ substrate for lower voltages than in the active area of the diode. Therefore, W' is the width of the base or n-type region of the diode under the guard ring. The breakdown voltage dependence on W' and doping density N_D is shown in Fig. 6.

Another important consideration for determining realistic breakdown voltages is associated with the radius of curvature of the guard ring junction profile. Small radii can result in enhanced fields which lead to reduced breakdown voltages. For the class of guard ring profiles used in the present model, the radius of curvature is essentially equal to the depth of diffusion of the guard ring into the n-type epitaxial layer. (See Fig. 3.) The dependence of breakdown voltage on curvature for various doping densities is shown in Fig. 7. In order to insure the maximum
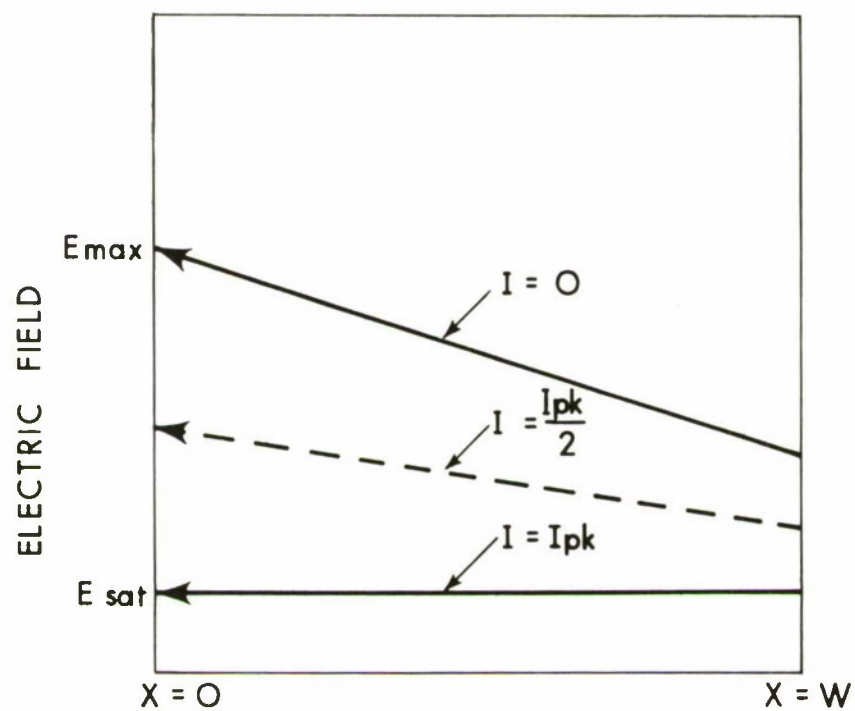
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Fig. 5. Electric field versus distance in EBS diode base region for $V \approx V_{BD}$.
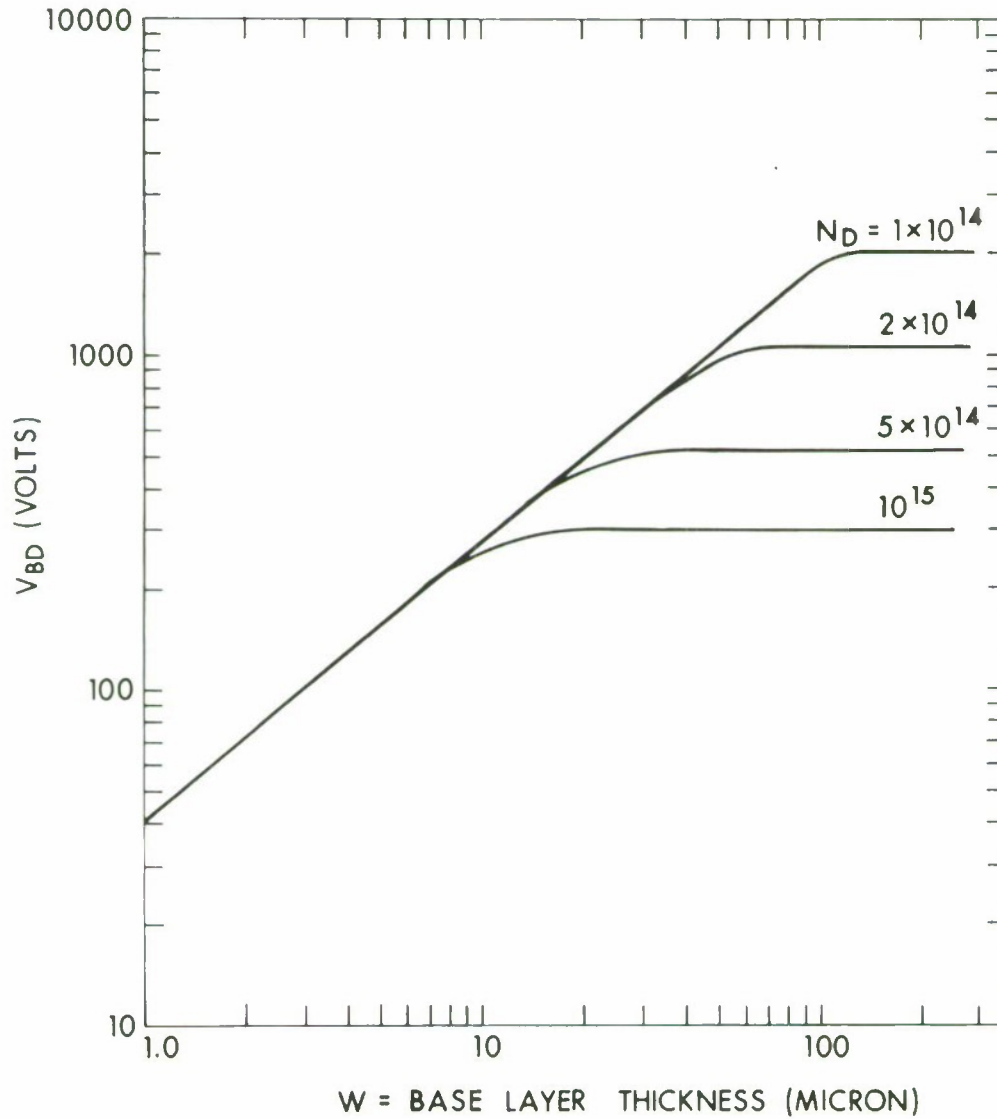
Fig. 6. Breakdown voltage versus diode thickness for p^+nn^+ diode.
(S. M. Sze and G. Gibbons, "Avalanche of Abrupt and Linearly Graded p-n Junctions in Ge, Si GaAs, and GaP," Appl. Phys. Letters 8, 111 [1966])
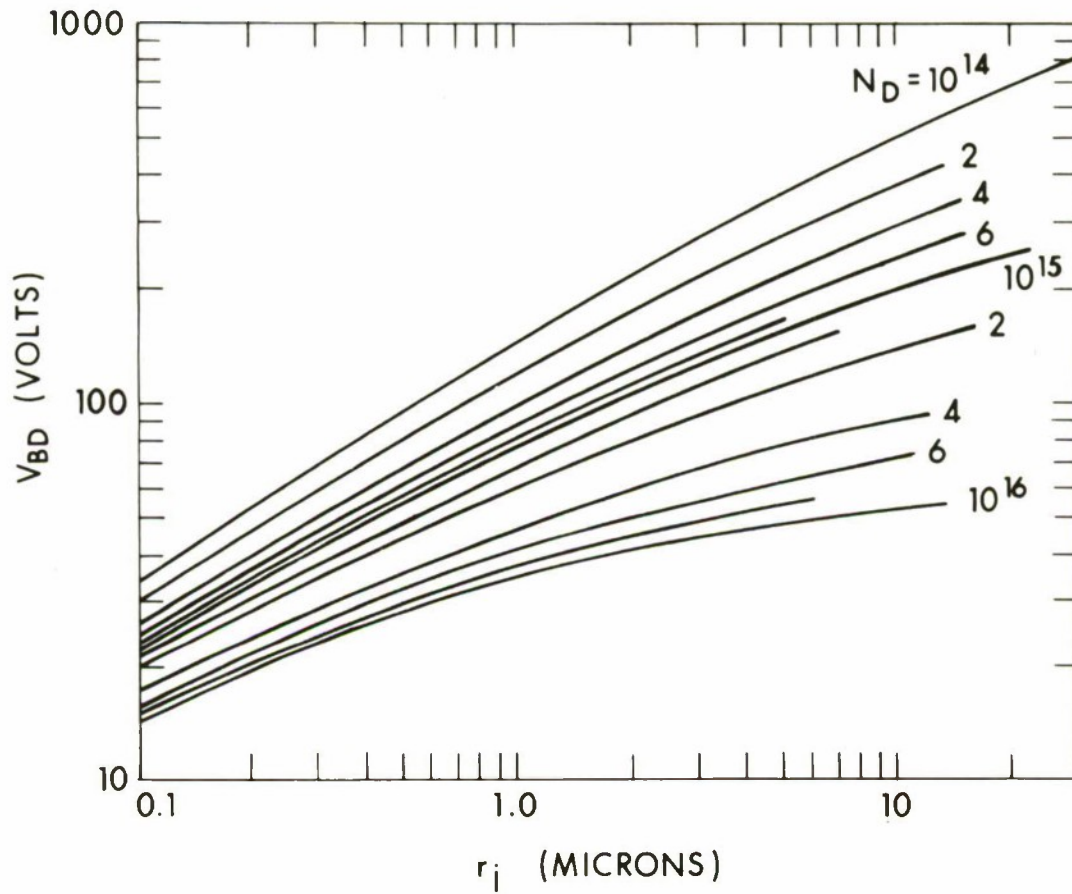
Fig. 7. Breakdown voltage versus junction radius of curvature, abrupt cylindrical junctions in silicon.
(S. M. Sze and G. Gibbons, "Effects of Junction Curvature on BD Voltages in p-n Junctions, "Solid-state Electronics 9, 831 [1966])

12

breakdown voltage for a given epitaxial layer thickness, the depth of the guard ring junction must be adjusted critically.   The total epitaxial thickness W_e is determined by the active region thickness W and the shallow junction depth W_j:

$$W_e = W + W_j. \tag{6}$$

Likewise, the total epitaxial width is equal to the sum of the guard ring radius r_j and the base width under the guard ring W´:

$$W_e = r_j + W´ \tag{7}$$

and, therefore,

$$W = r_j + W´ - W_j. \tag{8}$$

The maximum available breakdown voltage versus W for various doping densities based on the limits of Figs. 6 and 7 are shown in Fig. 8.   For the simple diode geometry designs which require no guard ring structures such as a mesa diode, the breakdown voltage (V_{BD}) would be determined by letting W = W´ in Fig. 6.

With V_{min} and V_{BD} or V_{max} as restrictions on the peak-to-peak RF voltage swing, the total voltage across the diode is visualized as shown in Fig. 9 where a sinusoidal waveform is used for convenience and assumed symmetrical about a DC bias voltage V_B.   The RF power output density (per unit diode active area) of the EBS target at the fundamental frequency is the product of the RMS values of the sinusoidal fundamental components of voltage and current density:

$$p_o = V_{rms} \cdot J_{rms}. \tag{9}$$

Since we are considering a tuned output amplifier, all frequency components of voltage, except the fundamental frequency, see a short circuit load and, therefore,
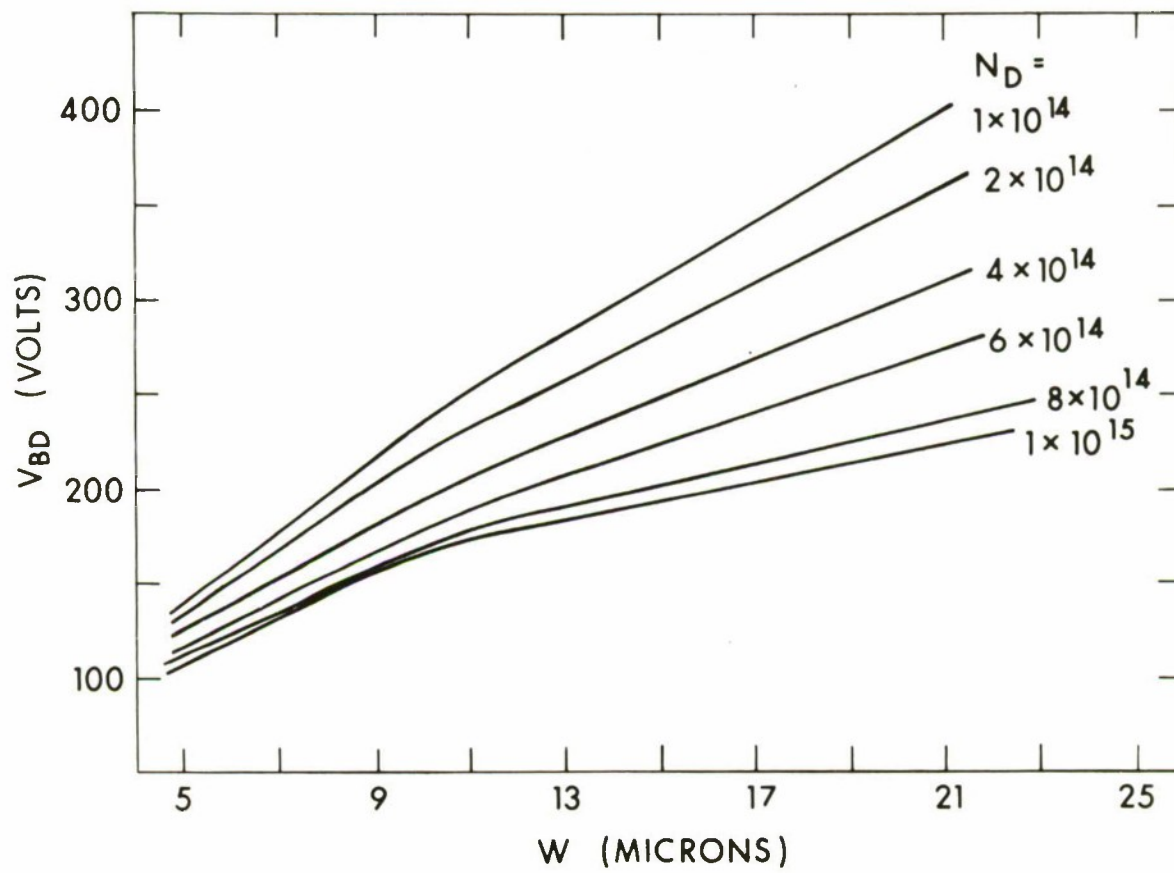
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Fig. 8. Breakdown voltage versus diode thickness including guard ring effects.
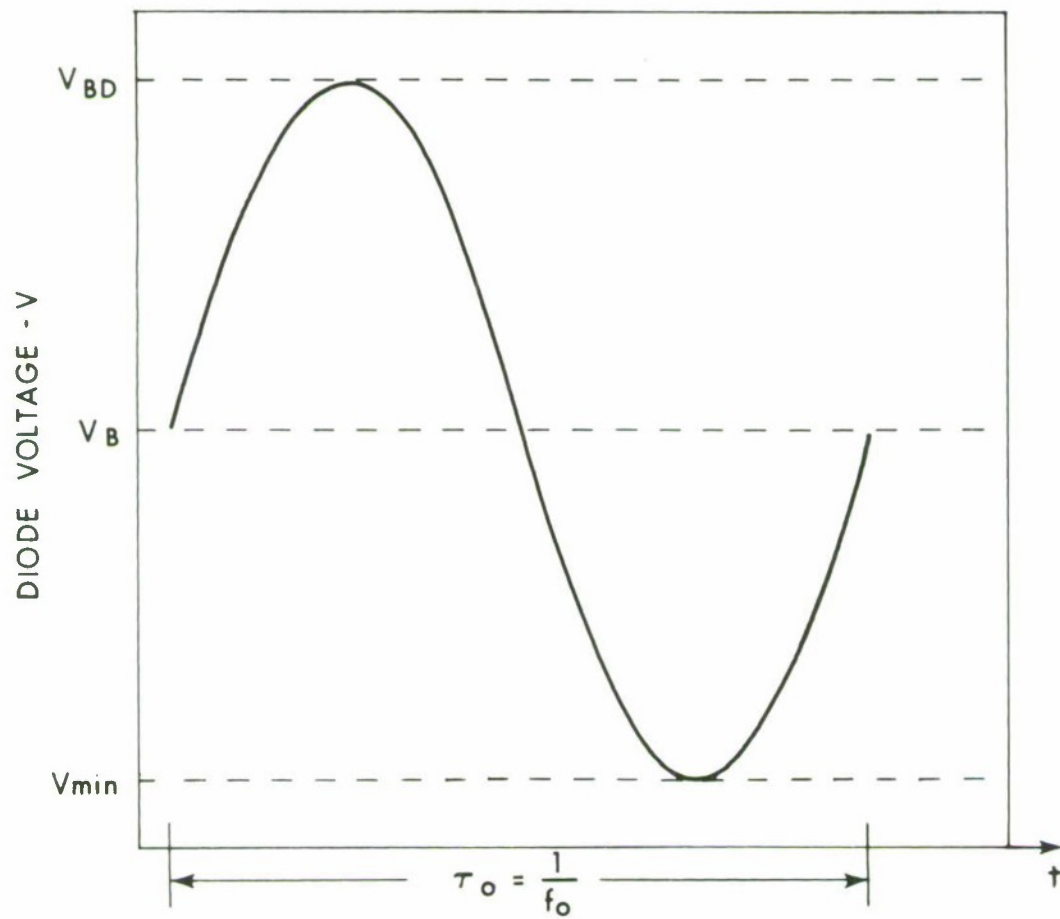
Fig. 9. Diode voltage waveform.

$$V_{rms} = \frac{V_{max} - V_{min}}{2\sqrt{2}} \qquad (10)$$

as in Fig. 9.

The non-sinusoidal current waveform is limited to a maximum value J_{pk} as defined above. J_{pk} is related to the maximum or peak value of the magnitude of the fundamental Fourier component of the non-sinusoidal waveform J_1 by

$$m = \frac{|J_1|}{J_{pk}} \qquad (11)$$

where m will be derived in Section 2.3 as a function of actual beam current density and diode current waveforms.

Therefore,

$$J_{rms} = \frac{m J_{pk}}{\sqrt{2}} \qquad (12)$$

and

$$p_o = \frac{(V_{max} - V_{min}) \, m J_{pk}}{4} \, . \qquad (13)$$

For practical considerations, the output of the EBS amplifier can be represented by a RF current source in shunt with the diode capacitance C and a load resistance R_L as shown in Fig. 10. The circuit Q for this parallel network is

$$Q = \omega_o C R_L \qquad (14a)$$

where ω_o = center frequency in radians. The capacitance of the diode active area with a correction for parasitic (fringing or stray) capacitance is

$$C = \frac{\varepsilon \varepsilon_o K A}{W} \qquad (14b)$$
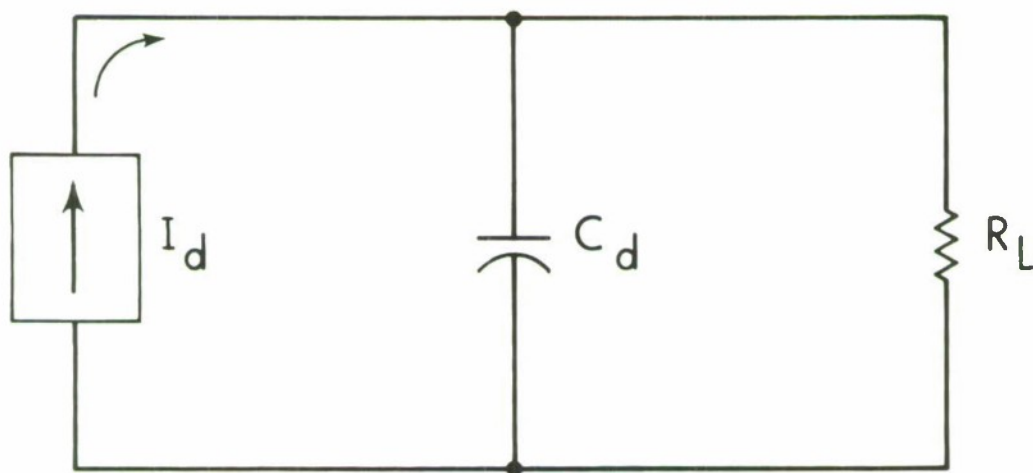
Fig. 10.   EBS diode equivalent circuit.

where

ϵ = relative permittivity of semiconductor material

ϵ_o = permittivity of free space

W = diode junction depletion width as defined above in Eq. (8)

K = correction factor which accounts for stray capacitance

A = diode active area.

The optimum load resistance R_L derived from the ratio of Eq. (10) to Eq. (12) is

$$R_L = \frac{V_{max} - V_{min}}{2m J_{pk} A} \qquad (14c)$$

Restrictions on the value for diode active area A based on thermal dissipation requirements are discussed in Section 2.4 below. The loaded Q of the diode target would be

$$Q = \frac{\omega_o \epsilon \epsilon_o (V_{max} - V_{min}) K}{2 W m J_{pk}} \qquad (15)$$

2.2 Waveforms and Device Efficiency

The primary application of the present EBS design model is for high power, high efficiency amplification of microwave power. Therefore, of greatest interest is a model which includes analysis of the non-linear waveforms associated with essentially Class-C operation. In general, this mode of operation requires that the RF current waveforms exist for a small fraction of the total period of the desired frequency. The non-sinusoidal current waveform has a frequency spectrum rich in harmonics which must be terminated with the appropriate impedances at each frequency. Since the maximum performance is required at the fundamental frequency or over a fractional bandwidth centered at this frequency, an output waveform efficiency can be defined which relates the RF output current at the fundamental frequency to the average value of the current waveform. This efficiency factor must be considered in conjunction with an efficiency associated with the diode

18

RF voltage restrictions, and an efficiency which accounts for overall input-output power requirements such as electron-beam power and filament power.

In this section a diode current waveform efficiency factor will be derived based on the two major time dependent mechanisms. First, the amount of time that the beam is on the target active area (τ_b) as compared to the time associated with the period of the fundamental or output frequency of operation (τ_o) is a strong influence on the total output current waveform. Second, the time required for carriers (electrons) to move across the base region of the diode under the applied electric field (τ_d) provides a limitation on the maximum size of the fundamental period. In the analysis below, expressions for diode current waveform will be derived based on these two time-dependent mechanisms. The efficiency factors for each case are found by using these time functions which derive the currents at the fundamental frequency and the DC or average components. A relationship between these efficiency factors is formulated which describes τ_b as a function of τ_d for maximization of device output capability and overall efficiency.

The following analysis uses a gaussian function to represent the beam or input current waveforms in order to derive these efficiency factors, relating them to the device material and geometry parameters. The basic amplifier model employs deflection of the beam on and off the diode target rather than an intensity modulation. This is a preferred modulation scheme because the beam deflection mechanism can be simply configured to provide an impedance match for the amplifier input circuitry.[4] Also, the possibility of deflecting the beam between two diode targets and thereby doubling the output power of the amplifier tube is attractive for some applications. The frequency or deflection rate is the center or fundamental frequency of interest. By adjustment of the degree of over-deflection (that is, varying the input RF drive power), the ratio of time-of-beam-on-target τ_b to total signal period $\tau_o = 1/f_o$ can be controlled, thus, determining the width of the beam current-on-diode

19

pulse length. A useful and fairly accurate representation of the beam current density distribution radially in space is a two-dimensional gaussian profile. For a rectangular or circular diode geometry, the dynamic superposition of the beam density distribution onto the diode active area leads to a beam current-on-diode pulse waveform which can be approximated by a gaussian waveform as shown in Fig. 11 as

$$I_b(t) = I_{b-pk} e^{-\frac{1}{2}(\frac{t}{\sigma_b})^2} \tag{16}$$

where σ_b = time value for 63 percent of peak amplitude.

The results of this analysis can also be applied to beam density or velocity modulation schemes which would provide an approximate gaussian waveform.

For the gaussian representation, τ_b is defined as the time width of the beam current pulse at one-half peak amplitude. This implies that τ_b is related to σ_b by

$$\tau_b = 2\sqrt{2\ln2}\,\sigma_b. \tag{17}$$

In order to account for transit-time effects on the diode output current waveform, it is convenient and adequate to represent the diode with a system or transfer function as shown in Fig. 12a and 12b. The response of this system function to an impulse delta-function input gives the diode output current as a function of transit time, τ_d. The transit-time, τ_d, is defined as the time required for the predominant current carrier (electrons for p+n diodes) to transit the active diode base region of length W at the saturation velocity or scattering limited velocity, v_{scl}:

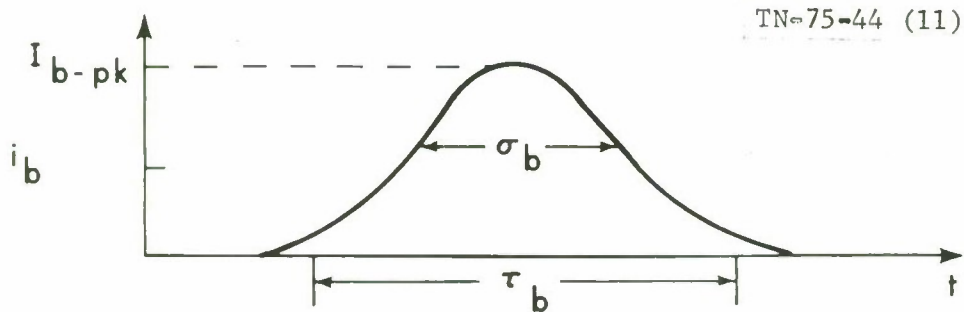$$\tau_d = \frac{W}{v_{scl}}. \tag{18}$$
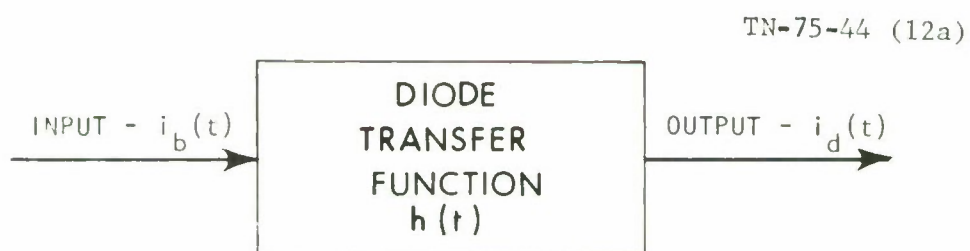
Fig. 11. Beam current on target waveform.

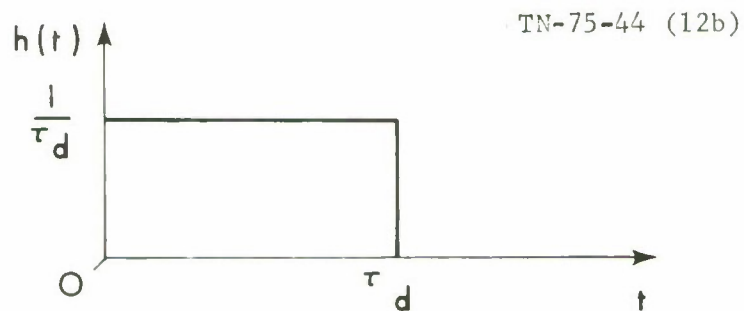Fig. 12a. Diode signal flow diagram.

Fig. 12b. Diode transfer function.

21

For the beam current input function $i_b(t)$ and the diode transfer function $h(t)$, the convolution of $i_b(t)$ and $h(t)$ yields the output diode current $i_d(t)$ or

$$i_b(t) * h(t) = i_d(t) \tag{19}$$

where $*$ = convolution.

Also, the output of the device as related to $i_d(t)$ is maximized if the normalized waveforms $i_b(t)$ and $h(t)$ are as similar as possible if not identical. For the present case, amplitudes as well as the values of τ_d and τ_b with respect to τ_o are, therefore, specifically interrelated to provide maximum output and highest waveform efficiency.

The total waveform efficiency is directly proportional to the efficiency of the individual waveforms associated with the diode transit-time response as shown in Fig. 12b and the beam time-on-target as shown in Fig. 11. In general, a waveform efficiency can be defined[5] for a tuned output device as,

$$\eta = \frac{|I_1|}{2I_{DC}} \tag{20}$$

where $|I_1|$ = magnitude of the fundamental frequency component of the waveform
I_{DC} = DC or average value of the waveform.

For the gaussian waveform associated with the input or beam current on diode $i_b(t)$, the fundamental component of the Fourier transform is

$$I_1(\omega) = \frac{\omega_o}{2\pi} \int_{-\infty}^{\infty} I_{b\text{-pk}} \, e^{-\frac{1}{2}\left(\frac{t}{\sigma_b}\right)^2} e^{-j\omega_o t} \, dt \tag{21}$$

22

Solving this integral yields,

$$|I_1(\omega)| = I_{b\text{-pk}} \frac{2\sqrt{2\pi} \, \sigma_b}{\tau_o} e^{-(\sqrt{2\pi} \, \sigma_b/\tau_o)^2} \qquad (22)$$

where,

$$\tau_o = \frac{1}{f_o} = \text{period of the fundamental frequency}$$

$$\tau_b = \text{(defined in Eq. (17) above).}$$

The DC or average value of $i_b(t)$ is found by solving

$$I_{DC} = \frac{2I_{b\text{-pk}}}{\tau_o} \int_o^{\tau_o/2} e^{-\frac{1}{2}(\frac{\tau}{\sigma_b})^2} dt \qquad (23)$$

which yields

$$I_{DC} = I_{b\text{-pk}} \frac{\sqrt{2\pi} \, \sigma_b}{\tau_o} . \qquad (24)$$

The waveform efficiency of the beam current is, therefore,

$$\eta_g = \frac{|I_1|}{2I_{DC}} \qquad (25)$$

or

$$\eta_g = e^{-(\sqrt{2\pi} \, \sigma_b/\tau_o)^2} . \qquad (26)$$

For the transit-time response waveform efficiency, the fundamental component of the rectangular response waveform is found from

23

$$I_d(\omega) = \frac{\omega_o}{\pi} \int_{-\infty}^{\infty} \frac{I_o}{\tau_d} e^{-j\omega_o t} \, dt \tag{27}$$

to be

$$|I_1| = \frac{2}{\tau_d} \frac{\sin \frac{\omega_o \tau_d}{2}}{\frac{\omega_o \tau_d}{2}} I_o. \tag{28}$$

The DC average value of $i_d(t)$ is

$$I_{DC} = \frac{I_o}{\tau_d} . \tag{29}$$

The rectangular pulse efficiency is, therefore,

$$\eta_r = \frac{|I_1|}{2I_{DC}} \tag{30}$$

or

$$\eta_r = \frac{\sin \frac{\omega_o \tau_d}{2}}{\frac{\omega_o \tau_d}{2}} . \tag{31}$$

In terms of τ_o (to be consistent with Eq. (26) above),

$$\eta_r = \frac{\sin \frac{\pi \tau_d}{\tau_o}}{\frac{\pi \tau_d}{\tau_o}} \tag{32}$$

24

Based on the two efficiency terms derived above, a total or cascaded waveform efficiency can be represented by

$$\eta_w = \eta_g \bullet \eta_r \tag{33}$$

and is, therefore,

$$\eta_w = \frac{\sin \pi \tau_d / \tau_o}{\pi \tau_d / \tau_o} \bullet e^{- (\sqrt{2} \pi \sigma_b / \tau_o)^2}. \tag{34}$$

Since σ_b is a function of τ_b as defined by Eq. (17) above, η_w can be rewritten as

$$\eta_w = \frac{\sin \pi \tau_d / \tau_o}{\pi \tau_d / \tau_o} \bullet e^{- (\sqrt{2} \pi \tau_b / \tau_o \, 2\sqrt{2 \ln 2})^2}. \tag{35}$$

This expression, therefore, relates the total diode waveform efficiency to both τ_d and τ_b.

The next objective is to maximize this efficiency factor resulting in a specific optimum relationship between τ_d and τ_b. The approach which incorporates a rigorous mathematical treatment is addressed in Appendix 1. An approach which simplifies the analysis, resulting in a reasonably optimum relationship as shown in Appendix 1, is followed below. The simplifying assumption is based to some degree on qualitative reasoning. As pointed out above in the discussions associated with Eq. (19), maximum output is obtained if the normalized waveforms associated with $i_b(t)$ and h(t) are as identical as possible. Likewise, maximum efficiency would be desirable for the case where both time dependent mechanisms contribute equally to the overall device efficiency. Therefore, it will be assumed here and verified in Appendix 1 that reasonable optimization can be achieved for the situations where the individual waveform efficiences are equal, that is

25

$$\eta_g = \eta_r \, , \tag{36}$$

which relates τ_d to τ_b.

Therefore, from Eq. (26) and Eq. (32),

$$\frac{\sin \pi \tau_d / \tau_o}{\pi \tau_d / \tau_o} = e^{- (\pi^2 / 2) \, (1 / [2 \ln 2]) \, (\tau_b / \tau_o)^2} \, . \tag{37}$$

Solving for τ_b with respect to τ_d results in

$$\frac{\tau_b}{\tau_o} = \sqrt{- \frac{4 \ln 2}{\pi^2} \ln \left[\frac{\tau_o}{\pi \tau_d} \sin \pi \frac{\tau_d}{\tau_o} \right]} \tag{38}$$

A numerical solution is shown in the curve of Fig. 13 where it is apparent that a close fit approximation can be defined as

$$\tau_b = 0.69 \, \tau_d \, . \tag{39}$$

Since we have taken the case of $\eta_r = \eta_g$ above, the total waveform efficiency becomes

$$\eta_w = \eta_r \cdot \eta_g = \eta_r^2 = \eta_g^2 \, . \tag{40}$$

Arbitrarily choosing η_g^2 as the factor for formulation implies,

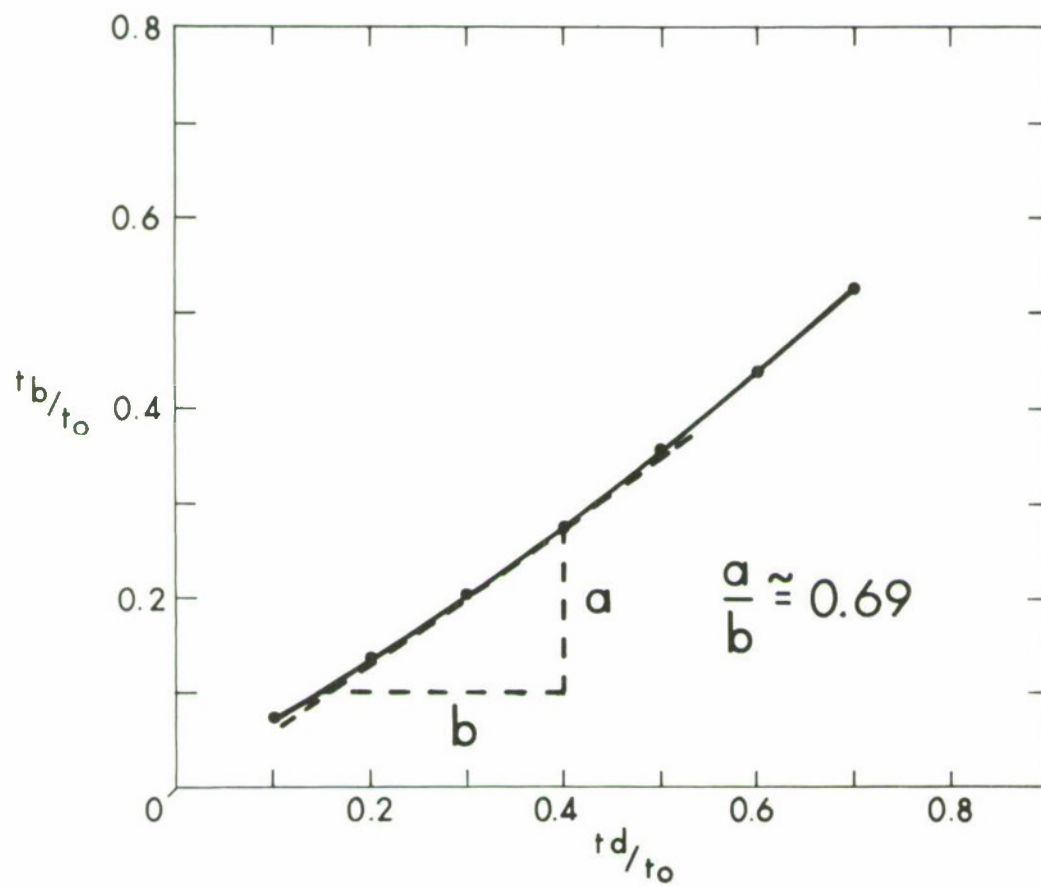$$\eta_w = \eta_g^2 = e^{- 2 (\sqrt{2} \pi \sigma_b / \tau_o)^2} \tag{41}$$

Fig. 13. τ_b versus τ_d for maximum efficiency.

or

$$\eta_w = e^{-3.39 \, (\tau_d/\tau_o)^2}. \tag{42}$$

Before considering the other efficiency factors associated with the diode and overall amplifier, it is convenient at this point to derive the waveform factor m, which has been used previously in Section 2.2 to determine output power density and circuit Q. The waveform factor for the diode output,

$$m = \frac{|I_1|}{I_{pk}} = \frac{AJ_1}{AJ_{pk}} \tag{43}$$

includes the magnitude of the fundamental component of the diode output current I_1. A rigorous calculation of this current component would require the operations of Eq. (19) to get $i_d(t)$ and finally a transform to the frequency domain for I_1. In order to simplify the calculations, it is assumed, at this point, that, since the normalized waveforms of $i_b(t)$ and h(t) are quite similar for maximum output requirements, the output current waveform would be near gaussian in shape with a σ_d equal to approximately $\sqrt{2} \, \sigma_b$ of the input gaussian waveform, that is,

$$i_d(t) = I_{d-pk} \, e^{-\frac{1}{2} \, (t/\sigma_d)^2} \tag{44}$$

where $\sigma_d = \sqrt{2} \, \sigma_b$.

This assumption is rigorously verified on page 35 of Ref. 6. Taking the Fourier transform of Eq. (44) yields at the fundamental frequency,

$$I_1 = I_{d-pk} \, \frac{2\sqrt{2\pi} \, \sigma_d}{\tau_o} \, e^{-(\sqrt{2} \, \pi \, \sigma_d/\tau_o)^2} \tag{45}$$

28

The waveform factor m is then,

$$m = \frac{I_1}{I_{d-pk}} = \frac{4\sqrt{\pi}\,\sigma_b}{\tau_o}\, e^{-2(\sqrt{2}\,\pi\,\sigma_b/\tau_o)^2} \,. \tag{46}$$

According to Eq. (41),

$$m = \frac{2\sqrt{\pi}\,\sigma_b}{\tau_o}\,\eta_w \tag{47}$$

or

$$m = 0.69 \sqrt{\frac{2\pi}{\ln 2}} \left(\frac{\tau_d}{\tau_o}\right) \eta_w = 2.077 \left(\frac{\tau_d}{\tau_o}\right) \eta_w \,. \tag{48}$$

Another important efficiency factor is the intrinsic diode efficiency associated with the diode target relating to the available voltage swing across the diode terminals during an RF period. The limitations on voltages as discussed in Section 2.2 above are the breakdown voltage mechanisms and the minimum voltage necessary to maintain scattering limited velocity for the carriers, (see Fig. 9). This intrinsic diode efficiency accounts for the realistic condition that the E_{sat} electric field must be maintained resulting in a finite V_{min}. The intrinsic diode efficiency is defined as

$$\eta_i = \frac{V_{max} - V_{min}}{V_{max} + V_{min}} \tag{49}$$

which is a function of the device material and thickness as shown in Section 2.1. The total diode efficiency or cascaded efficiency, therefore, would be

$$\eta_d = \eta_w \cdot \eta_i \,, \tag{50}$$

or

$$\eta_d = \left(\frac{V_{max} - V_{min}}{V_{max} + V_{min}} \right) e^{-3.39 \, (\tau_d/\tau_o)^2}. \tag{51}$$

The previous analysis has considered the efficiency factors associated only with the semiconductor diode portion of the EBS device. In order to apply the present analysis to the design of EBS devices to satisfy specific systems requirements, efficiency factors which include power inputs to the electron beam must also be included. An overall efficiency factor is defined as,

$$\eta = \frac{P_o}{P_{in}}, \tag{52}$$

where P_o = RF output power per unit diode area, P_{in} = total DC input power per unit diode area.

The input power is composed of DC power to the diode target $P_d(DC)$ plus high voltage power associated with the beam $P_b(DC)$. As pointed out above, beam current on the diode target is modulated by RF deflection of the beam on and off the target. For this mode of operation, DC power is continuously provided to the beam. If grid modulation of the beam current or grid gating of the beam in addition to deflection is used, then a different and higher overall efficiency is realized since the beam power is required for only portions of the RF output cycle. Therefore, two overall efficiency factors are of interest,

$$\eta_{min} = \frac{P_o}{\frac{1}{\eta_o} P_o + P_b} \tag{53}$$

30

$$\eta_{max} = \frac{P_o}{\frac{1}{\eta_o} P_o + P_b'} \tag{54}$$

where P_b = static beam power, P_b' = gated beam power.

Proceeding with the derivations of P_b and P_b', it will be assumed that approximately one half of the current of the gaussian shaped beam falls on the diode active area when the beam is centered on the diode. The total beam power per unit diode area is

$$P_b = \frac{1}{2} \frac{I_b}{2\pi R^2} V_{acc} \tag{55}$$

where R = radius of diode active area, V_{acc} = accelerating beam voltage. The beam current density which is radially gaussian can be represented by

$$J_b = \frac{J_{pk}}{C_1 M} e^{-(1/2)(r/\sigma_b)^2} \tag{56}$$

where M = static beam current multiplication factor (see Fig. 2), and C_1 = reduction factor for M due to the short time that the beam is on the diode target during RF cycle.

The total beam current is then

$$I_b = \int_o^\infty \int_o^{2\pi} \frac{J_{pk}}{C_1 M} e^{-(1/2)(r/\sigma_B)^2} r \, dr \, d\theta \tag{57}$$

31

which yields,

$$I_b = \frac{J_{pk}}{C_1 M} 2 - \sigma_B^2 . \tag{58}$$

The value of σ_B for the gaussian current distribution and the condition that half the beam current falls on an area of radius R is

$$\sigma_B = 0.85 \text{ R}. \tag{59}$$

Therefore,

$$I_b = 2 - (0.722)R^2 \frac{J_{pk}}{C_1 M} . \tag{60}$$

The dynamic gain reduction factor C_1 arises since the factor M is only the DC or average current gain of the diode target, this is

$$\hat{I}_d = M\hat{I}_b . \tag{61}$$

For Eq. (60), the peak current values are employed in order to incorporate the J_{pk} term which relates the basic physical and geometric parameters as described in Eq. (2); and, therefore, the gain reduction factor C_1 modifies the average gain factor M to a waveform sensitive current gain factor. Convolving the normalized waveform $i_b(t)$ and $h(t)$ at the point of peak response results in the normalized output waveform factor which is, actually, the waveform sensitive factor C_1.

$$I_{pk} = M\hat{I}_b [i_b(t) * h(t)] \tag{62}$$

$$I_{pk} = \frac{\hat{I}_b M}{\tau_d} \int_{-\tau_d/2}^{\tau_d/2} e^{-(1/2)(\tau/\sigma_b)^2} \, dt. \tag{63}$$

Using Eqs. (17) and (39), τ_d is related to σ_b by

$$\sigma_b = \frac{0.69}{2\sqrt{2\ln 2}} \, \tau_d. \tag{64}$$

Therefore, solving (63) above,

$$I_{pk} = 0.67 \, \hat{I}_b M \tag{65}$$

or $C_1 = 0.67$.

Using Eqs. (60) and (55), the total beam power per unit diode area becomes,

$$P_b = (0.722) \frac{J_{pk}}{0.67 M} V_{acc}. \tag{66}$$

This would be applied to the efficiency factor η_{min} as in Eq. (53). For the maximum efficiency factor η_{max}, the average beam power is reduced for the case when there is no beam power while the beam is not on the diode target. That is, the beam is gated "on" for some time period τ' which is related to the time width of the gaussian beam current-on-diode waveform τ_b. This time on target τ' with respect to the period τ_o results in a duty factor which acts to reduce the total beam input power. For a normalized gaussian waveform, such a duty factor, is the average value of the waveform divided by the peak. Therefore, taking the value of τ' for the average value of the gaussian waveform, it can be shown that[7]

33

$$\tau' = \sqrt{2\pi} \, \sigma_b \, . \tag{67}$$

Using Eqs. (17) and (39), one obtains for a duty factor, D. F.,

$$\text{D. F.} = \frac{\tau'}{\tau_o} = (1.07) \, \frac{\tau_b}{\tau_o} \tag{68}$$

or

$$\text{D. F.} = 0.734 \, \frac{\tau_d}{\tau_o} \, . \tag{69}$$

It is apparent from Eq. (68) that the value of τ' is very close to τ_b as would be expected for a maximized output device.

Allowing for an initial assumption that approximately one half the beam current falls on the diode active area, the form of the gated beam power becomes from Eq. (66),

$$P_b' = (1/2) \, (0.734 \, \frac{\tau_d}{\tau_o}) \, P_b \, . \tag{70}$$

The two overall effeciency factors Eqs. (53) and (54) become

$$\eta_{min} = \frac{P_o}{\dfrac{P_o}{\eta_D} + 2.15 \, \dfrac{J_{pk}}{M} \, V_{acc}} \tag{71}$$

and

$$\eta_{max} = \frac{P_o}{\dfrac{P_o}{\eta_D} + 0.789 \, \dfrac{\tau_d J_{pk}}{\tau_b M} \, V_{acc}} \, . \tag{72}$$

34

Having derived the beam power on diode, it is appropriate to derive the total power dissipated in the diode target per unit diode area;

$$P_d = \left(\frac{1 - \eta_d}{\eta_d} \right) P_o + P_b', \tag{73}$$

or

$$P_d = \left(\frac{1 - \eta_d}{\eta_d} \right) P_o + (0.789) \frac{\tau_d J_{pk}}{\tau_o M} V_{acc}. \tag{74}$$

2.3 Thermal Dissipation Analysis

In order to establish a complete design model for EBS RF amplifiers, consideration must be given to possible applications requiring long pulse length, high duty factor, or CW operation; all of which require a finite amount of power to be dissipated in the semiconductor diode target. In Section 2.3 above, an expression for the total power dissipation density in the diode target [Eq. (74)] was derived based on various design parameters of the diode and electron beam. In this section, the capability of a diode target of finite geometry to transfer the dissipated heat to an attached heat sink in order to maintain an elevated but safe temperature of operation will be addressed. In general, for a constant upper temperature limit, the higher the output power density available (also the power dissipation density), the smaller the diode active area must be. This implies that the practical output power capability of a diode target is limited by low impedance restrictions associated with the device capacitance and bandwidth requirements as well as the thermal restrictions associated with the device dissipation capability. This is because both phenomena are related to the diode active area.

In the following section, a model will be described which leads to an expression for the maximum active area of the diode target as a function of power dissipation density, maximum safe temperature of operation, and other geometric and thermal factors.

35

The thermal model which applies has been described in detail in Ref. 8. In order to simplify the analysis, certain initial conditions have been assumed as listed below:

a) The diode is assumed infinitely thin, which implies that there is no temperature difference between the exposed surface and the heat sink surface of the diode chip. (This approximation is realistic since EBS diodes can be reduced in thickness to a few mils for typical diameters or widths of 50 to 100 mils.)

b) The heat sink for calculation purposes is assumed to be semi-infinite in dimension and with zero temperature at the boundaries. In practice, a relatively large heat sink with convection or water cooling can provide this condition.

c) Since the diode is assumed thin, the highest temperature will be at the center of the circular diode or heat sink area.

d) The heat dissipation in the diode active volume for a thin diode can be represented by a uniform heat flux density q impinging on the diode area $A = \pi R^2$.

The diagram of Fig. 14 illustrates some of the previous initial conditions. In Ref. 9, the general heat conduction differential equation is solved and an expression for this particular geometry is derived for the time dependent temperature as a function of various parameters as shown in Eq. (75)

$$\Delta T = \frac{2q}{K} \left(\frac{St}{\pi} \right)^{1/2} \left[1 - \exp\left(\frac{R}{2\sqrt{St}} \right)^2 + \sqrt{\pi} \frac{R}{2\sqrt{St}} \left(1 - \mathrm{erf}\left(\frac{R}{2\sqrt{St}} \right) \right) \right] u(t) \quad (75)$$

where ΔT = temperature rise above zero

  K = thermal conductivity of heat sink

  S = thermal diffusivity

  R = radius

  t = time

  u(t) = unit step function.

36

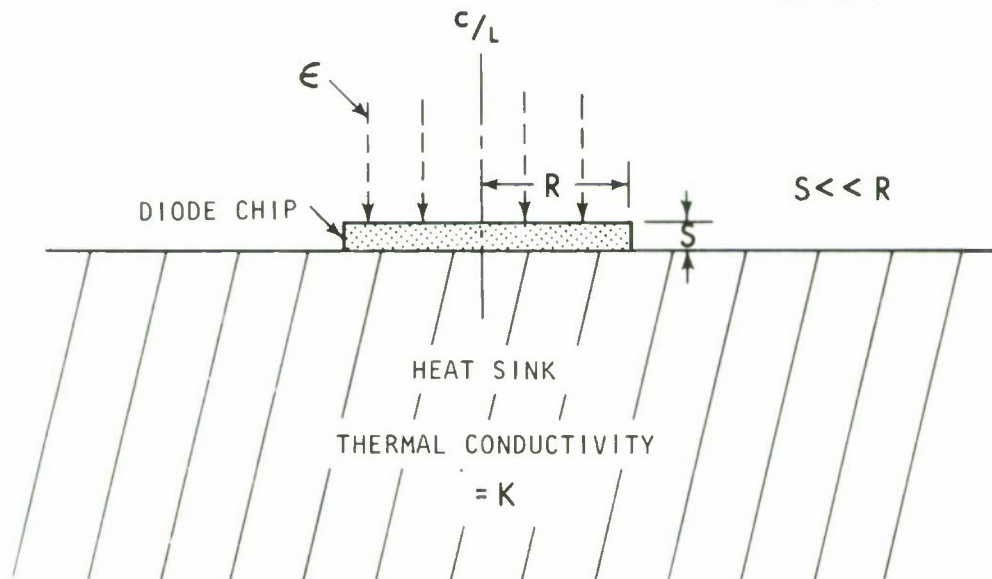Fig. 14. Heat flow geometry for diode-heat sink interface.

For the present analysis dealing with CW operation, as $t \to \infty$, Eq. (75) reduces to:

$$\Delta T = \frac{qR}{K} . \tag{76}$$

The total heat flux, Q, is

$$Q_T = q \pi R^2 . \tag{77}$$

Solving Eq. (76) for ΔT using Eq. (77) yields

$$\Delta T = \frac{Q}{K \pi R} .$$

The thermal spreading impedance associated with the geometry is then

$$\theta_S = \frac{\Delta T}{Q_T} = \frac{1}{K \pi R} . \tag{79}$$

The total thermal impedance of the diode heat sink system is composed of θ_S plus a contribution θ_C from the semiconductor chip of finite thickness, plus θ_B, which is associated with the thermal conductivity properties of the chip to heat sink bond.

$$\theta_T = \theta_S + \theta_C + \theta_B . \tag{80}$$

For this analysis $\theta_C \to 0$.

The thermal impedance of the bond for dimensions typical to those of the EBS diode target have been found experimentally to be approximately 0.68°C/watt. (Unpublished results at General Radio Company, Concord, Massachusetts.)

The total power dissipated in the diode target is

38

$$P_D' = \frac{\Delta T}{\theta_T} = \frac{\Delta T}{\theta_B + \frac{1}{K \pi R}} \ . \tag{81}$$

Solving for ΔT as a function of power dissipation density, P_D,

$$\Delta T = \theta_B P_D A + \frac{P_D}{\sqrt{\pi} K} \sqrt{A} \ . \tag{82}$$

The solution to this equation for maximum area A and a finite temperature rise is

$$A = \left[\sqrt{\left(\frac{1}{2 \theta_B \sqrt{\pi} K} \right)^2 + \frac{\Delta T}{\theta_B P_D}} - \frac{1}{2 \theta_B \sqrt{\pi} K} \right]^2 \tag{83}$$

where, in summary,

θ_B =   thermal impedance of chip to heat sink bond

K =   thermal conductivity of heat sink material

P_D =   power dissipation density

ΔT =   maximum allowable temperature rise above ambient.

2.4   Amplifier Circuit Design

A complete EBS amplifier design procedure must include consideration of parameters associated with the input and output circuits of the amplifier in addition to those of the active device which have been presented above. The performance capabilities are primarily limited by the power dissipation capability and the available or realizable circuit impedances for a specific frequency and bandwidth requirement. For the general case, EBS devices require both input and output impedance matching networks. In the present design model, the input matching

requirement are not addressed. It is assumed that microwave power tube circuit techniques are available to enable the input power to effectively provide RF grid modulation of the beam or that RF beam deflection techniques are available such as described in Ref. 4.

The output impedance matching network can be designed starting with the equivalent circuit representation of the diode plus package as shown in Fig. 15. The output network is needed to resonate or tune-out all reactive elements of the equivalent circuit at the desired frequency and bandwidth as well as to transform the value of the external load impedance (usually 50Ω) to the required optimum load impedance R_L derived previously in Eq. (14c) above. The network must also provide a low RF loss, and a DC path in order to bias the diode to V_B.

For most practical EBS devices, the series diode resistance R_D of Fig. 15 can be restricted to values less than $0.1\ \Omega$ by thin metalization of the diode active area as well as high quality multiple lead contacts. Also, lead inductance, L_D, can be made insignificant using microwave packaging techniques such as ribbon-shaped multiple parallel leads. Therefore, the equivalent circuit of Fig. 15 can, in practice, be reduced to a current source shunted by a total capacitance C_T which is the sum of C_d and C_p.

For this circuit, the impedance matching requirements are very similar electrically to those developed for microwave power transistor collector circuits. Depending on frequency of interest, either lumped components or distributed network (transmission line) techniques apply. Present applications emphasize UHF through S-band frequencies for which neither approach is clearly superior. Experience indicates that lumped element circuit designs fabricated in strip line or microstrip networks are the most practical (providing the widest range of realizable impedances).

The total capacitance, C_T, is normally resonated with a series or shunt inductive
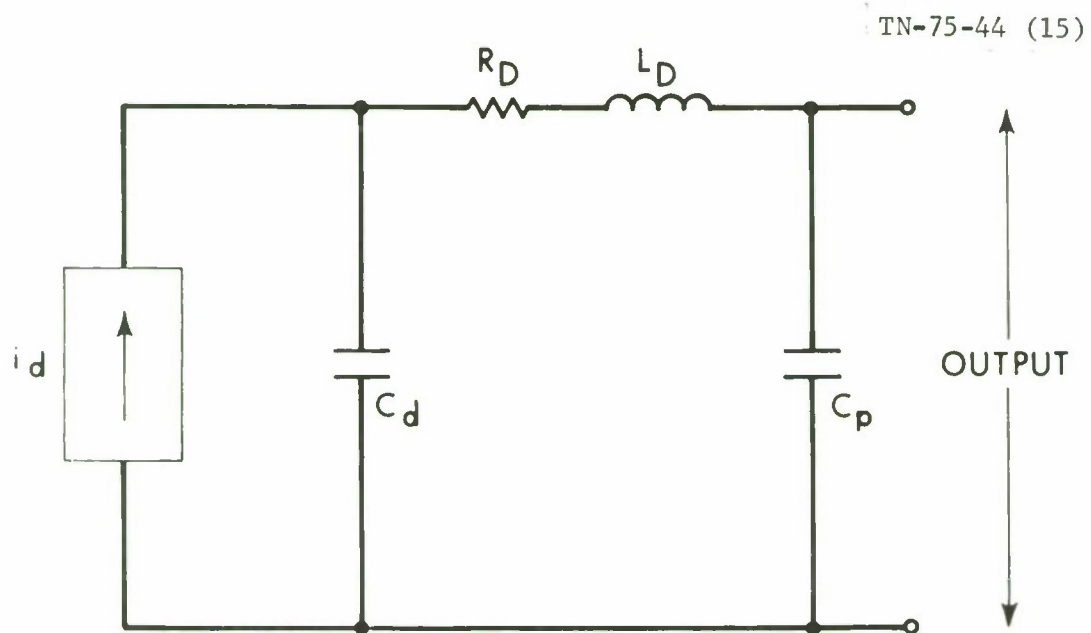
Fig. 15.   EBS diode plus package equivalent circuit.

element L_1 as shown in Fig. 16. The impedance transformation can be realized by several design techniques, [10] the simplest of which would be "L," "π," or "T" voltage divider networks, evolving to more complex filter networks for greater pass-band shaping, and finally, transmission line elements such as quarter wave transformers. A highly desirable circuit arrangement exists when the value of the total capacitance, C_T, is such that it can be incorporated as the initial component in the design of simple or more complex filter networks which provide the transformation. This condition reduces the number of independent reactive elements resulting in improved bandwidth control and reduced circuit loss.

Physically the circuit design problems are more demanding for EBS devices than for transistors. The networks should be located adjacent to the diode chip which requires, for most uses, that they be positioned within the vacuum tube structure precluding all possibility of circuit adjustment during operation to maximize performance. There-fore, the circuits must be fabricated of high dielectric constant materials for minaturization or small components all of which must not outgas in order to maintain high quality vacuums as well as survive high temperature (350°C or more) vacuum bake out for tube processing. Therefore, simple networks fabricated in ceramic microstrip, typically alumina, with appropriate conductor metalization, such as moly-chrome, are of practical interest.

A summary of the generalized design procedure would be:

1. For a specific amplifier performance requirement, use the design formulas of Sections 2.1, 2.2, 2.3, and 2.4 above to determine the resultant values of R_L and C_T.

2. Design the output networks for R_L and C_T using approaches referred to above.

3. Determine if components of the network are realizable using lumped
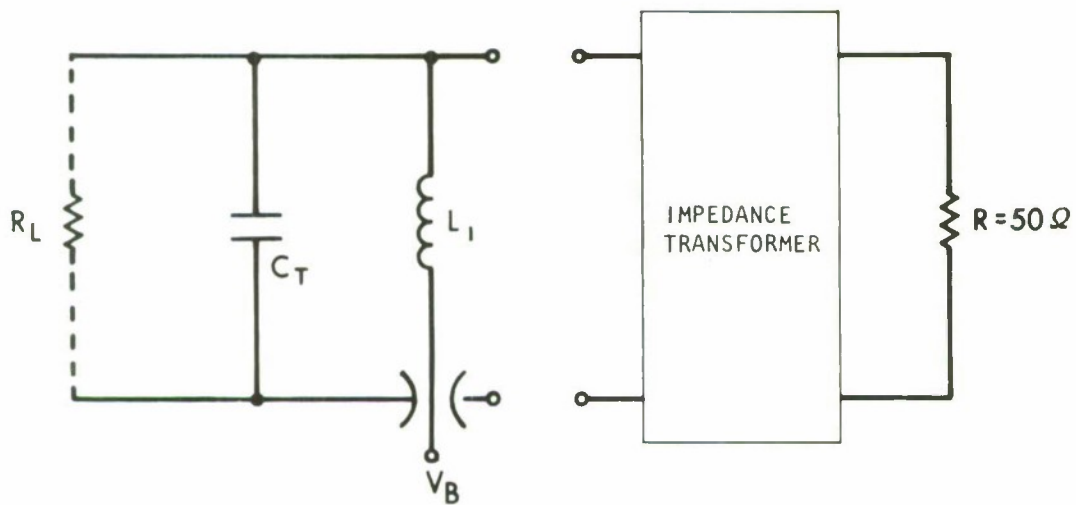
a) Independent DC bias terminal
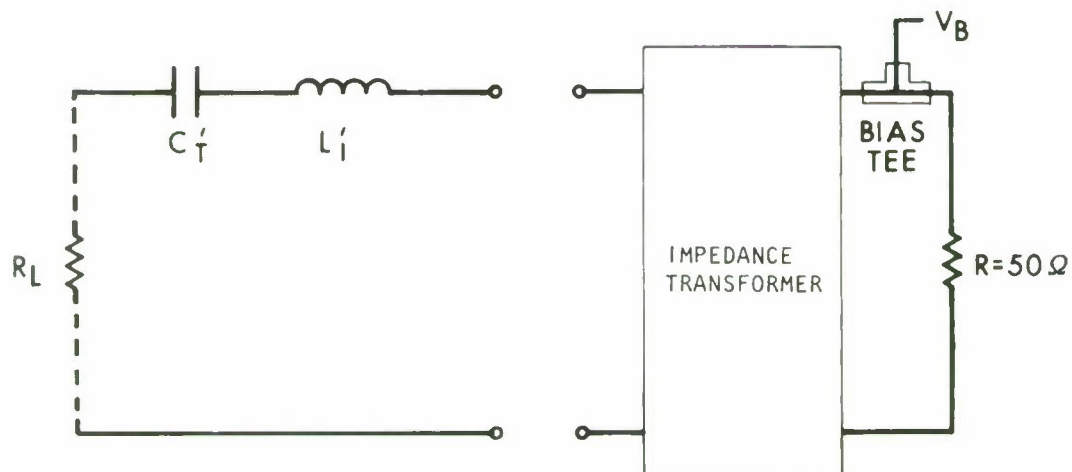
TN-75-44 (16b)

$C_T{}' = $ SERIES EQUIVALENT OF C_T

$L_1{}' = $ SERIES EQUIVALENT OF L_1

b) Diode bias through output port.

Fig. 16.   EBS diode output networks.

43

or distributed network techniques.

4.   If networks are not realizable, perform tradeoffs in performance requirements to obtain realizable circuit requirements.

3.0   Design Criteria Summary

A summary of the amplifier design relationships is presented below for convenience in applying the dynamic analysis to high power EBS amplifier designs. Several initial conditions have been established to make feasible the above analysis and should be considered in employing the complete design model.

1.   The waveform analysis is based on the beam current-on-diode being essentially gaussian in shape and as a function of time. Abnormal beam cross section current densities and diode active area geometries would require somewhat different driving functions in the analysis.

2.   The analysis deals with an amplifier employing only one diode target. Multi-target devices would provide improved performance; however, different beam current-on-diode functions and thermal dissipation characteristics are required for the analysis.

3.   Prime power supplied to the electron gun cathode heater filament has not been included in the analysis.

4.   In the analysis subsection dealing with the time of minimum voltage swing (V_{min}), a conservative value for the minimum electric field of 35 kV/cm for silicon was assumed. In practice, a lower value of approximately 10 kV/cm would be acceptable resulting in a lower V_{min}, and therefore, somewhat higher output power P_o and device efficiences, η_i and η_D. The lower E_{min} results in some deterioration of device linearity; to no consequence, however, since Class-C waveforms have already negated the possibility of linear operation.

5.   As pointed out in the RF output circuit subsection, the present output circuit considerations are based on a specific diode packaging configuration. Other packaging techniques could require modification of the network considerations.

For the conditions above and the various semiconductor materials, electron beam, and operating requirement parameters as listed in Table I, the design formulas are as summarized in Table II.

4.0   S-band, CW-RF Amplifier

In this section the design criteria derived and summarized above will be applied to a specific amplifier to demonstrate the overall procedure as well as provide a practical example of the highly competitive performance capabilities of an EBS device.

A proposed application is for an S-band amplifier with a 10-percent bandwidth centered at 2.1 GHz which would provide 50 to 100 watts of CW power with the highest overall device efficiency possible. Other design inputs include a beam accelerating potential of 10 kV = V_{acc}, and a diode target fabricated in silicon which would also require a guard ring junction profile and e-beam shielding structures.[11] The choice for silicon for the semiconductor and oxygen-free copper for the heat sink leads to the set of input material constants listed in Table III.

A computer program has been used to generate the design curves presented in Figs. 17 through 23 where various performance and circuit parameters are shown as a function of the diode active region width W and impurity doping density, N_D, for a p+nn+ device. A comparison of the curves indicates that the parameters vary continuously and that only the minimum overall device efficiency η_{min} (Fig. 21) shows any optimum range. An important and not surprising design criteria is apparent from comparing the calculated diode active area capacitance (Fig. 22) with the other design curves. That is, the capacitance is a strong function of doping

45

TABLE I

DESIGN INPUT PARAMETERS

I.   Material Parameters

v_{scl} -   scattering limited velocity

E_{sat} -   electric field for scattering limited velocity

ϵ -   relative dielectric constant

K   -   heat sink thermal conductivity

θ_B -   thermal impedance of chip to heat sink bond

ΔT -   maximum device temperature rise

N_D -   semiconductor impurity density

M   -   intrinsic beam to diode current gain at some V_{acc}

II. Beam Parameter

V_{acc} -   electron beam accelerating potential

III. Dimensional Parameters

W   -   width of diode base region beneath diode active area

K   -   parasitic capacitance multiplier

$\tau_o = \dfrac{1}{f_o} = \dfrac{2\pi}{\omega_o}$ - period of center frequency of operation

TABLE II

DESIGN EQUATIONS

1) Diode peak current density

$$J_{pk} = q\,v_{scl}\,N_D \tag{2}$$

2) Diode minimum voltage

$$V_{min} = W\,E_{sat} \tag{1}$$

3) Diode maximum voltage

$$V_{max} = \text{(see Fig. 8)}$$

4) $$V_B = \frac{V_{max} + V_{min}}{2} \quad \text{(see Fig. 9)}$$

5) Diode charge transit time

$$\tau_d = \frac{W}{v_{scl}} \tag{18}$$

6) Fundamental current to peak current ratio

$$m = 2.077(\tau_d/\tau_o)e^{-3.39\,(\tau_d/\tau_o)^2} \tag{48}$$

7) Optimum diode load resistance

$$R_L = \frac{V_{max} - V_{min}}{2\,m\,J_{pk}\,A} \tag{14b}$$

8) Diode active area capacitance

$$C = \frac{\varepsilon\varepsilon_o\,K\,A}{W} \tag{14a}$$

TABLE II (continued)

9) Diode active area

$$A = \left[\sqrt{\left(\frac{1}{2\theta_B\sqrt{\pi}\,K} \right)^2 + \frac{\Delta T}{\theta_B\,P_D}} \; - \; \frac{1}{2\,\theta_B\sqrt{\pi}\,K} \right]^2 \qquad (83)$$

10) Diode output loaded

$$Q = \frac{\omega_o\,\epsilon\epsilon_o\,K\,(V_{max} - V_{min})}{2\,Wm\,J_{pk}} \qquad (15)$$

11) Diode efficiency

$$\eta_D = \left(\frac{V_{max} - V_{min}}{V_{max} + V_{min}} \right) e^{-3.39\,(\tau_d/\tau_o)^2} \qquad (51)$$

12) Output power density

$$P_o = \frac{V_{max} - V_{min}}{4}\,m\,J_{pk} \qquad (13)$$

13) Diode power dissipation density

$$P_d = \left(\frac{1 - \eta_D}{\eta_D} \right) P_o + (0.789) \left(\frac{\tau_d}{\tau_o} \right) \frac{J_{pk}\,V_{acc}}{M} \qquad (74)$$

14) Overall EBS amplifier efficiency with DC electron beam

$$\eta_{min} = \frac{P_o}{\dfrac{P_o}{\eta_D} + (2.15)\,\dfrac{J_{pk}\,V_{acc}}{M}} \qquad (71)$$

15) Overall EBS amplifier efficiency with gated electron beam

$$\eta_{max} = \frac{P_o}{\dfrac{P_o}{\eta_D} + (0.789) \left(\dfrac{\tau_d}{\tau_o} \right) \dfrac{J_{pk}\,V_{acc}}{M}} \qquad (72)$$

48

TABLE II (continued)

16) Beam time on target

$$\tau_b = 0.69\,\tau_d \tag{39}$$

17) Beam current density (Beam Area = Diode active area)
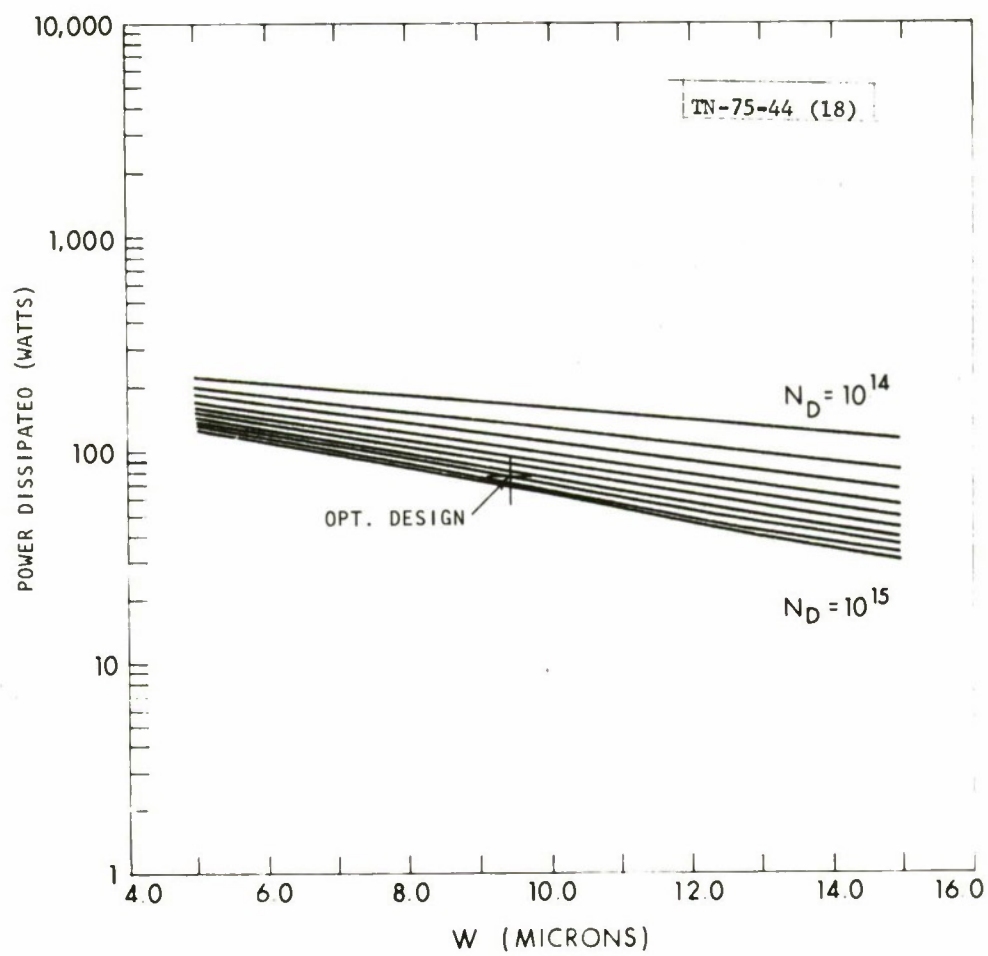
$$J_b = \frac{J_{pk}}{M} \tag{56}$$

TABLE III

MATERIAL PARAMETERS FOR S-BAND AMPLIFIER

v_{scl}	-	scattering limited velocity	$\underline{8 \times 10^6 \text{ cm/sec}}$
E_{sat}	-	electric field for scattering limited velocity	$\underline{3.5 \times 10^4 \text{ volts}}$
ε	-	relative dielectric constant	$\underline{12}$
K	-	heat sink thermal conductivity	$\underline{3.91 \dfrac{\text{watt.cm}}{\text{cm}^2 \, {}^\text{o}\text{C}}}$
θ_B	-	thermal impedance of chip to heat sink bond	$\underline{0.68 \, {}^\text{o}\text{C/watt}}$
ΔT	-	maximum device temperature rise	$\underline{190 \, {}^\text{o}\text{C}}$
M	-	intrinsic beam to diode current gain at same V_{acc}	$\underline{2000}$

Fig. 17. Output power versus diode thickness.

Fig. 18. Dissipated power versus diode thickness.

TN-75-44 (19)

80.

N_D DIODE EFFICIENCY

60.

OPT. DESIGN

$N_D = 10^{14}$

40.

$N_D = 10^{15}$

20.
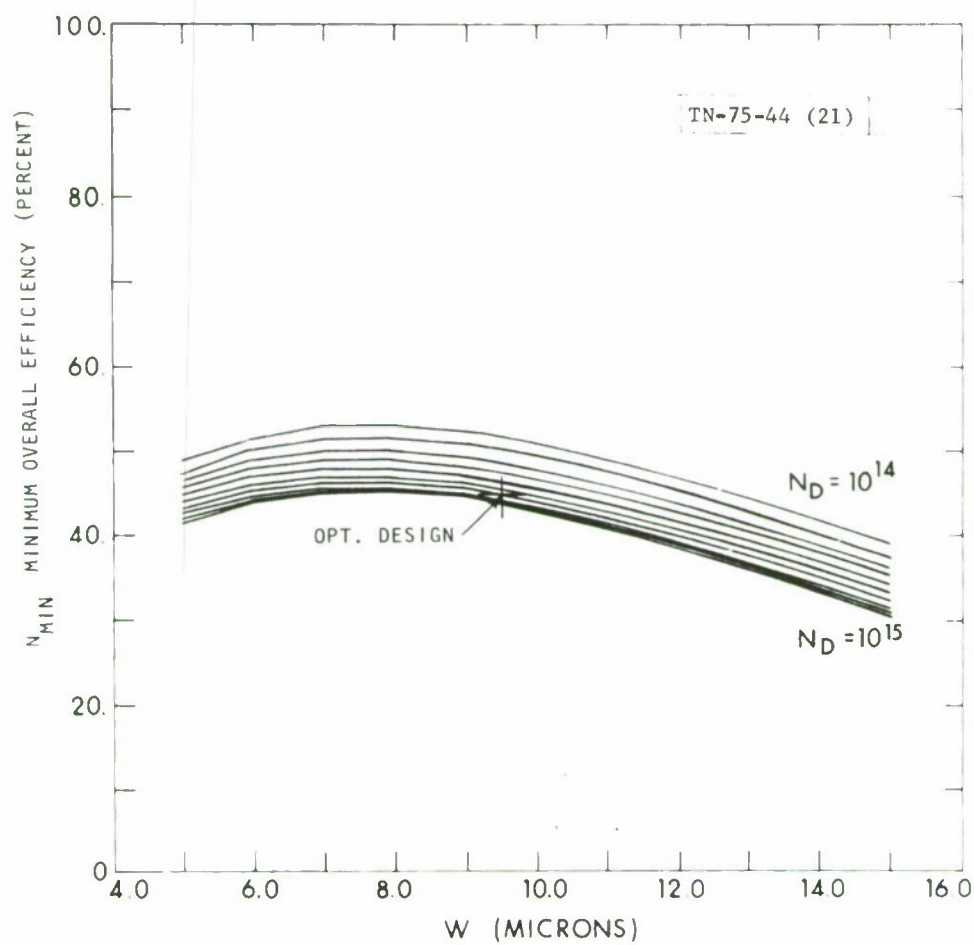
0
4.0   6.0   8.0   10.0   12.0   14.0   16.0

W (MICRONS)
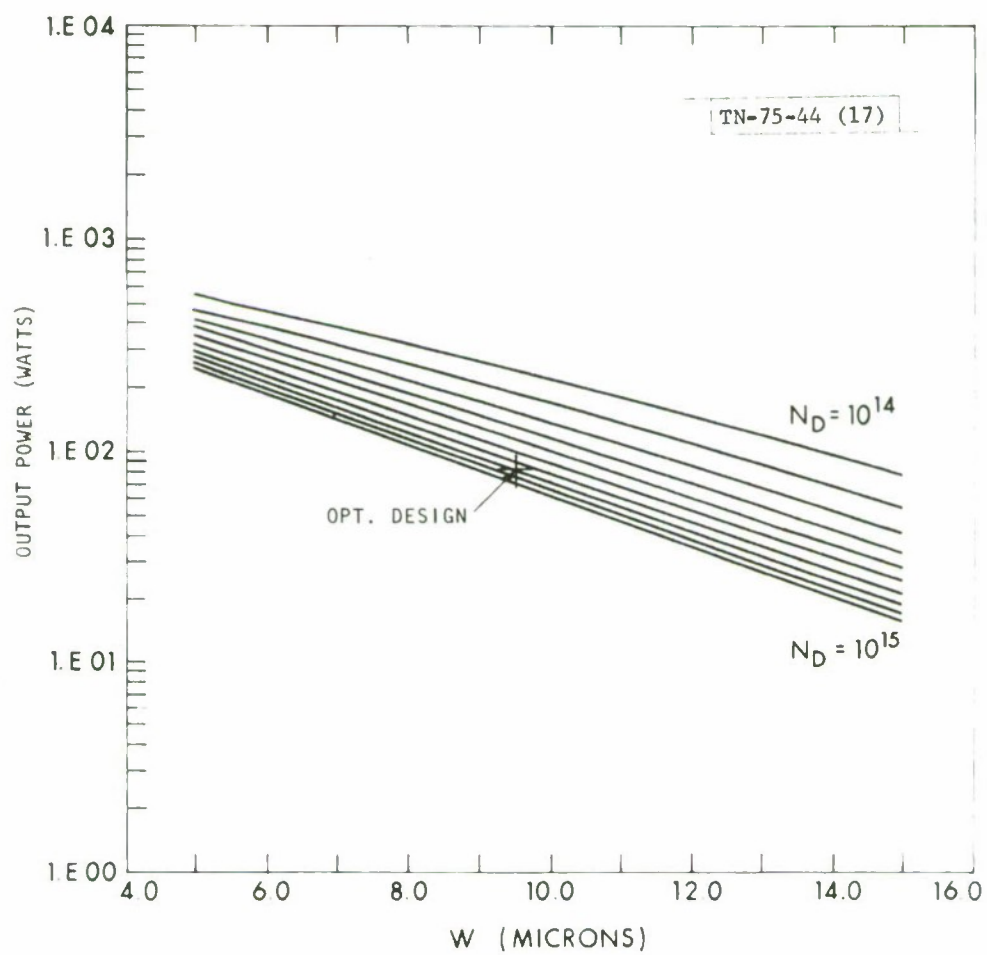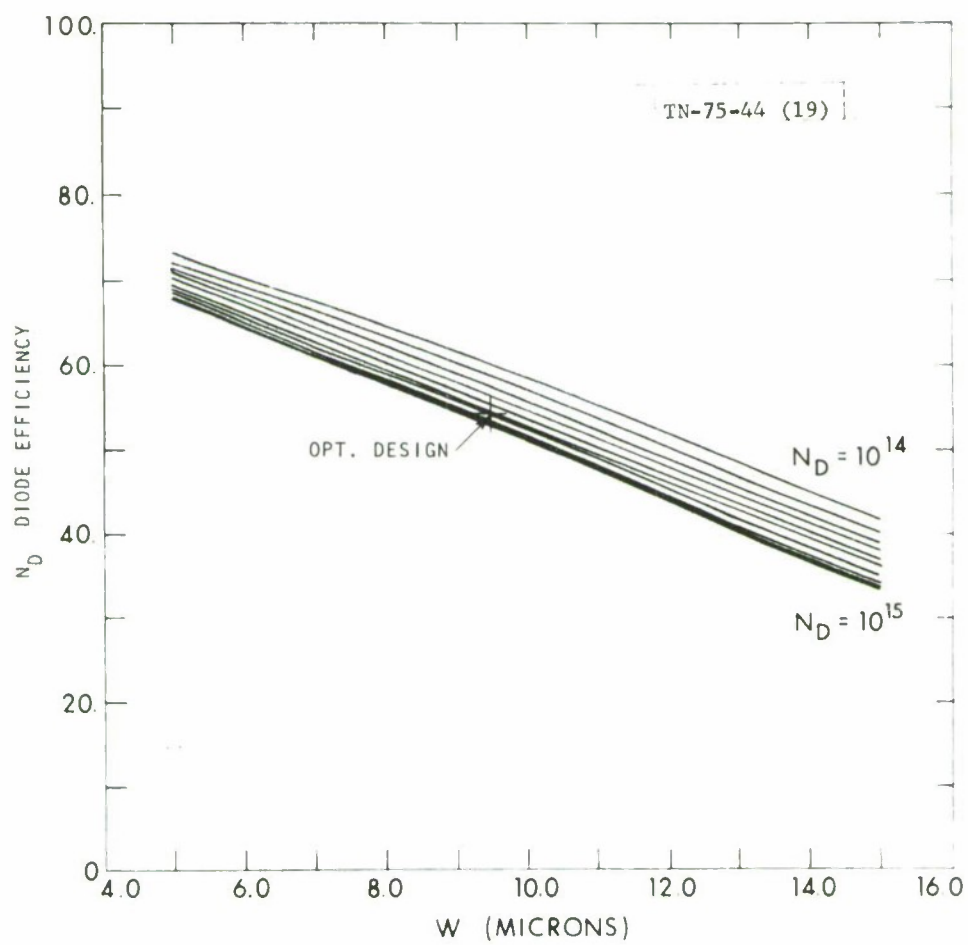
MATL: SI
F: 2100 MHz
TB/TD: 0.69

Fig. 19.   Diode efficiency versus diode thickness.
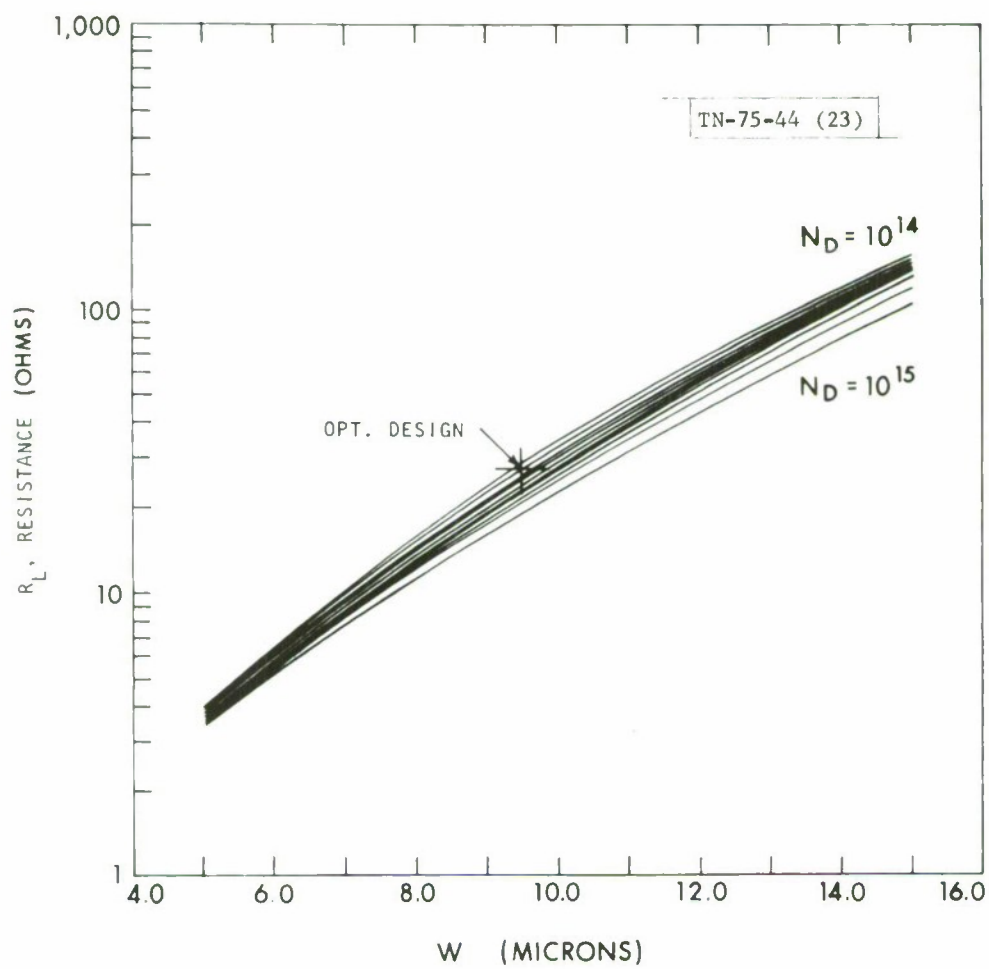
Fig. 20. Maximum efficiency versus diode thickness.

Fig. 21.   Minimum efficiency versus diode thickness.

Fig. 22. Capacitance versus diode thickness.

Fig. 23.   Resistance versus diode thickness.

density N_D and the higher the acceptable capacitance, the larger the output power and efficiency would be.

These characteristics can be used to sub-optimize (i.e., without a rigorous and detailed mathematical optimization calculation) a design which could achieve the desired requirements. A possible first step would be to choose candidate output impedance matching networks that are realizable for the highest possible values of diode capacitance C_D and load resistance R_L as related in curves of Figs. 22 and 23.

For this specific application example, the total capacitance C_T is virtually made up of the active area capacitance modified by a strong capacitance factor $K = 1.3$, C_D presented in Fig. 22, plus additional capacitance due to the junction guard ring structure and encapsulating RF package which amounts approximately to an additional 6 pf. Analysis of different circuit configurations indicates that for practically all candidates, a total capacitance of less than 13 pf would be necessary to achieve the desired bandwidth and permit circuit designs to be realizable. A final circuit design which incorporates the total capacitance C_T in a π matching filter network is shown in Fig. 24. A diode capacitance of 6.6 pf has been used which fixes the diode design at $W = 9.5 \mu$ and $N_D = 8.0 \times 10^{14}$ for reasonable output power and efficiency as shown by the indicator in Figs. 17 through 23. The total design specifications are listed in Table IV. The relative insensitivity of device performance to reasonable variations in diode geometry and material parameters control is illustrated in these design curves. This is a welcomed phenomena in the fabrication of any solid state device. The predicted performance is shown in Table V which indicates a desirable amplifier for the present application. A parallel design has been completed for the same application using GaAs. The device specifications and predicted performance are also shown in Tables IV and V.
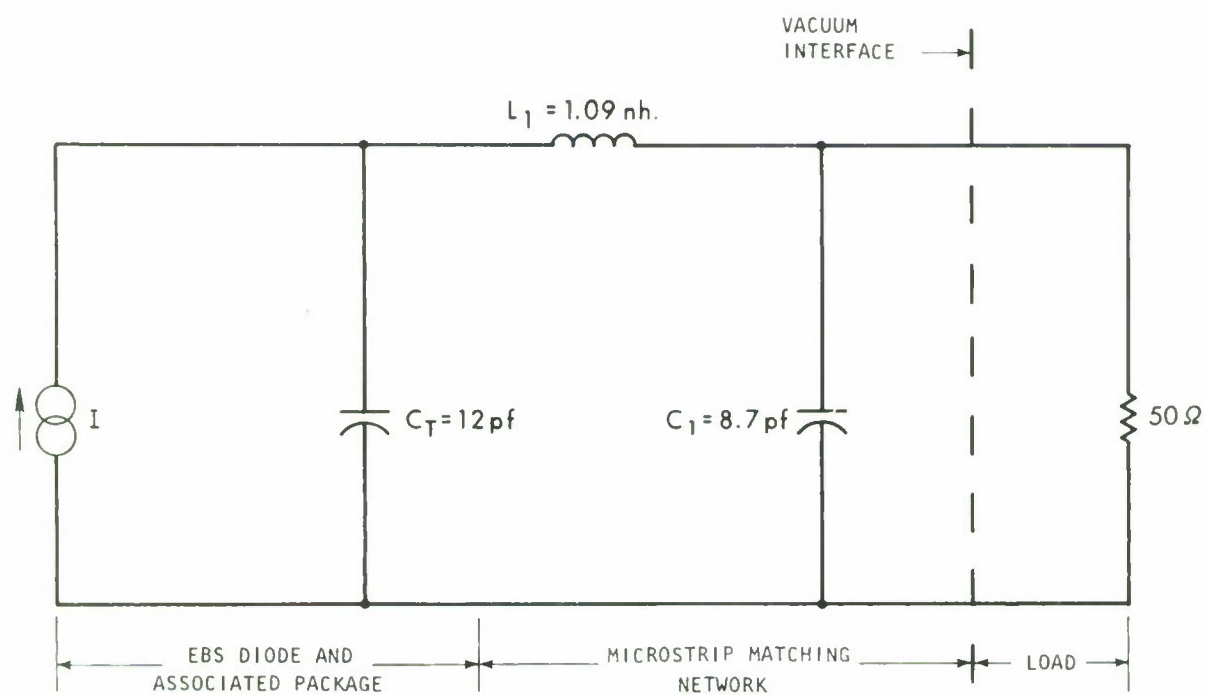
Fig. 24. EBS diode and matching network.

59

TABLE IV

DEVICE SPECIFICATIONS

A.   Silicon

-    Epitaxial planar diode, p+nn+ structure.

-    Epitaxial doping density, $N_D = 8 \times 10^{14}$ (n-type).

-    Active diode base width, W = 9.5 microns ± 10%.

-    p+ shallow diffusion depth of 0.3 microns ± 10%.

-    Active area of diode inside control region, A = 0.0059 cm^2 ± 10%.

-    Beam current requirement = 3.0 ma @ 10 kV.

B.   GaAs

-    Epitaxial proton bombarded diode.

-    Epitaxial doping density, $N_D = 8 \times 10^{14}$.

-    Active diode base width, W = 10 microns ± 10%.

-    Schottky barrier junction

-    Active area of diode inside control region, A = 0.0091 cm^2 ±10%.

-    Beam current requirement = 5.0 ma @ 10 kV.

TABLE V

PREDICTED PERFORMANCE

A.   Silicon

- F = 2100 MHz
- Power output - 82 watts CW
- Power gain = > 20 dB
- Load impedance = 25.6 Ω
- Diode power dissipation = 74 watts
- Frequency bandwidth = > 10%
- Amplifier efficiency (gated beam) = 52.3%

B.   GaAs

- F = 2100 MHz
- Power output - 132.4 watts CW
- Power gain = > 20 dB
- Load impedance = 23.5 Ω
- Diode power dissipation = 87 watts
- Frequency bandwidth = > 10%
- Amplifier efficiency (gated beam) = 60%

5.0 Conclusions

This report has presented the description of a comprehensive EBS RF amplifier design model which incorporated several constraints that evolve in the application of this device concept to practical amplifier requirements. An example amplifier has been designed leading to devices that were tested. A summary of the test results has been published separately.[12]

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APPENDIX 1

Equating Waveform Efficiency Functions

This appendix will rationalize the equating of the system efficiency function

$$\eta_{h(t)} = \frac{\sin(\pi \tau_d/\tau_o)}{\pi \tau_d/\tau_o}$$

to the gaussian beam pulse efficiency

$$e^{-(\sqrt{2}\pi \sigma_b/\tau_o)^2}$$

(as assumed in the main body of this technical report) for determination of an empirical relationship between τ_b and τ_d.

The overall efficiency of the beam diode interaction is determined by examining the output diode current pulse which is found by convolving the gaussian beam input with the system function. The assumption of equal efficiences;

$$\eta_{\substack{\text{diode} \\ \text{output}}} = \eta_{\substack{\text{gaussian} \\ \text{beam} \\ \text{input}}} \cdot \eta_{\substack{\text{system} \\ \text{function}}}$$

$$= \eta^2_{\substack{\text{gaussian} \\ \text{beam} \\ \text{input}}} = \eta^2_{\substack{\text{system} \\ \text{function}}},$$

leads to the empirical equation, $\tau_b = 0.69\,\tau_d$.

64

$$\left\{ \begin{array}{l} \eta_{\substack{\text{gaussian} \\ \text{beam} \\ \text{input}}} = e^{-\left(\sqrt{2}\,\pi\,\sigma_b/\tau_o\right)^2} = \dfrac{\sin \pi\tau_d/\tau_o}{\pi\tau_d/\tau_o} = \eta_{\substack{\text{system} \\ \text{function}}} \end{array} \right\}$$

Maximizing the diode output and the diode efficiency are the main objectives. These can be realized by adjusting the input gaussian beam and rectangular system function to provide equal contribution to the diode output and overall efficiency. It will be shown in this appendix that by equating the efficiency function

$$\left(\eta = \frac{I_1}{2I_{dc}} \right)$$

of each function, a reasonable optimization can be achieved.

Given a unity area gaussian function and rectangular function:
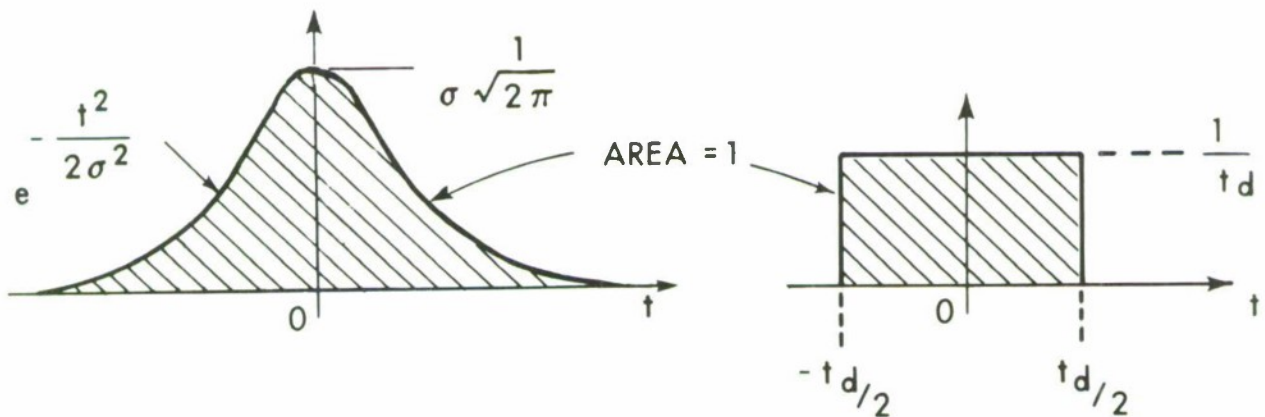
By superimposing the gaussian and rectangular functions given that $\tau_b = 0.69\tau_d$ and $\tau_b = 2.359\sigma_b = 2.359$ (for $\sigma_b = 1$) where τ_b is defined to be the width at 50 percent amplitude), the following graph is obtained:
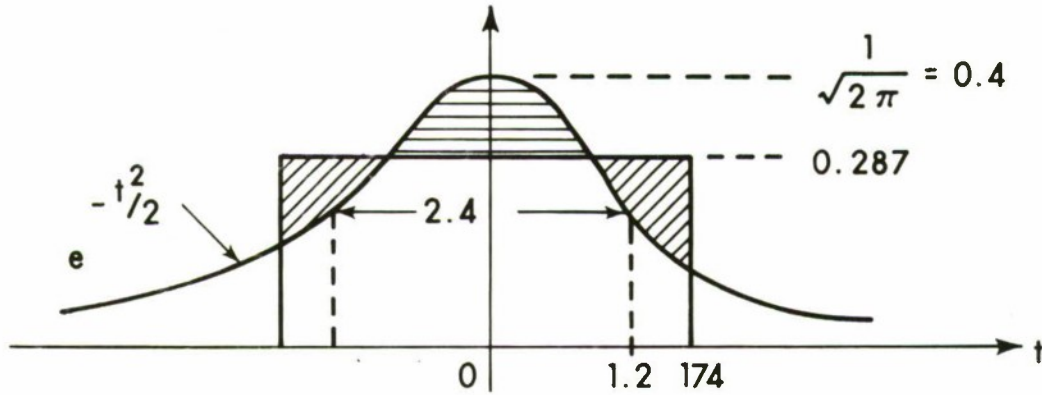
An error will exist since the functional fit is an approximation.

A computer program was written to generate output data by varying τ_b/τ_d ratios. All of the equations in the main body of the note remain the same with the exception of the following three equations:

$$\eta_{\text{diode output}} = \frac{\sin \pi \tau_d/\tau_o}{\pi \tau_d/\tau_o} \cdot e^{-(\pi^2/\ln 16)(\tau_b/\tau_d)^2 (\tau_d/\tau_o)^2} \tag{1}$$

66

$$m = \sqrt{\frac{2\pi}{\ln 2}} \left(\frac{\tau_b}{\tau_d} \right) \left(\frac{\tau_d}{\tau_o} \right) \eta_{\text{diode output}} \tag{2}$$

$$P_b = (0.722) \left(\frac{\tau_d}{\tau_b} \right) \left(\sqrt{\frac{\ln 2}{\pi}} \right) \frac{J_{pk} \cdot V_{acc}}{M \, \text{erf} \left(\frac{\tau_d}{\tau_b} \sqrt{\ln 4} \right)} \tag{3}$$

The following graphs will illustrate the dependence of various outputs of the system equations on the ratio, τ_b/τ_d. The graphs will be grouped into two sets.

The first set (W [thickness] = constant parameter for a series of N_d parametric curves) depict relative insensitivity of the various outputs to the ratio, τ_b/τ_d. Figure A.1, and A2 show that power output density and η_{min} increase with increasing τ_b/τ_d while in Fig. A3, η_{max} decreases with increasing τ_b/τ_d. (The slopes of the various curves can be approximated by a straight line with a small slope.) To choose an optimum τ_b/τ_d just from the graphs in set one, one would have to find an acceptable maximum, η_{max}, and minimum, η_{min}.

The second set of figures (N_d [doping density] = constant parameter for a series of W parametric curves) illustrates about the same degree of sensitivity of various outputs to τ_b/τ_d with the exception of the η_{min} curve. Figure A.4 shows a relative increase of the output power density with increasing τ_b/τ_d while Fig. A.5, a relative decrease.
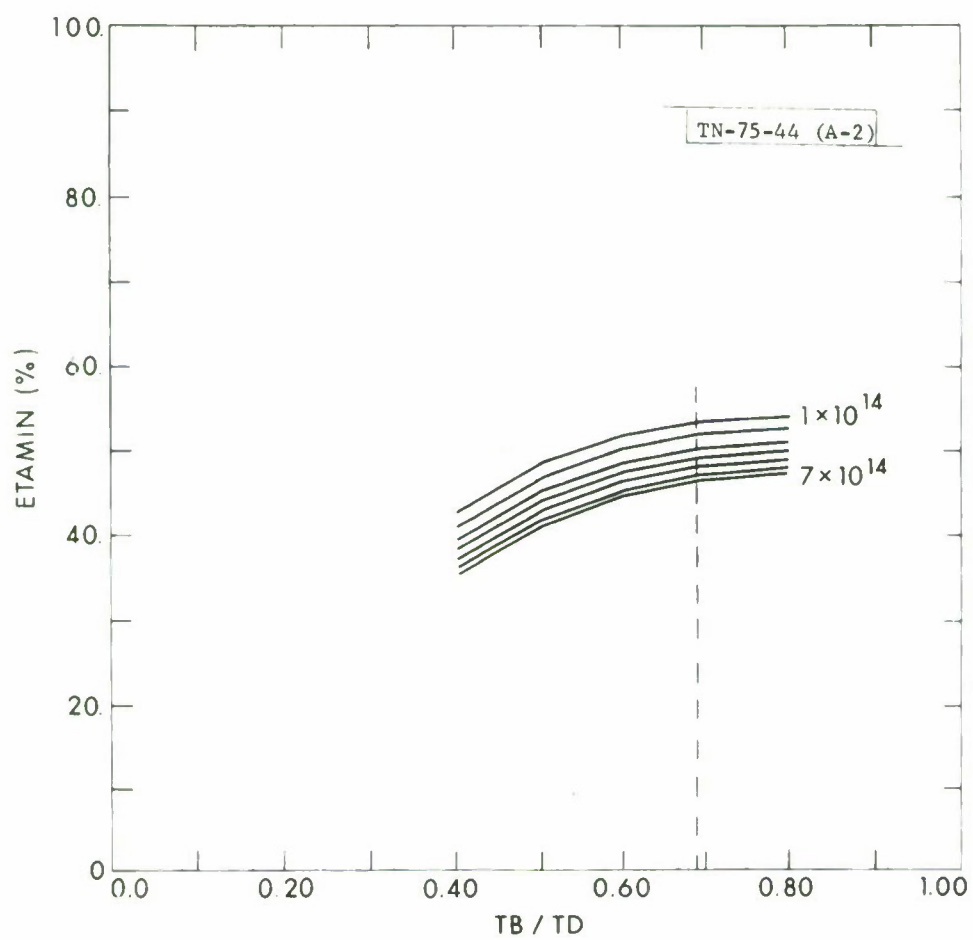
The curves A.6a and A.6b (η_{min} - curves) possess a distinct difference from the same curves found in set one. The curves in A.6a (5 → 8 microns) overlap with the curves in A.6b (9 → 15 microns). (Note the slope change between the curves in each graph.)

Choosing the ratio $\tau_b/\tau_d = 0.69$ proves to be a compromise. One can see that the optimum ratio is dependent on both N_d and W subject to acceptable η_{min} and η_{max} values.
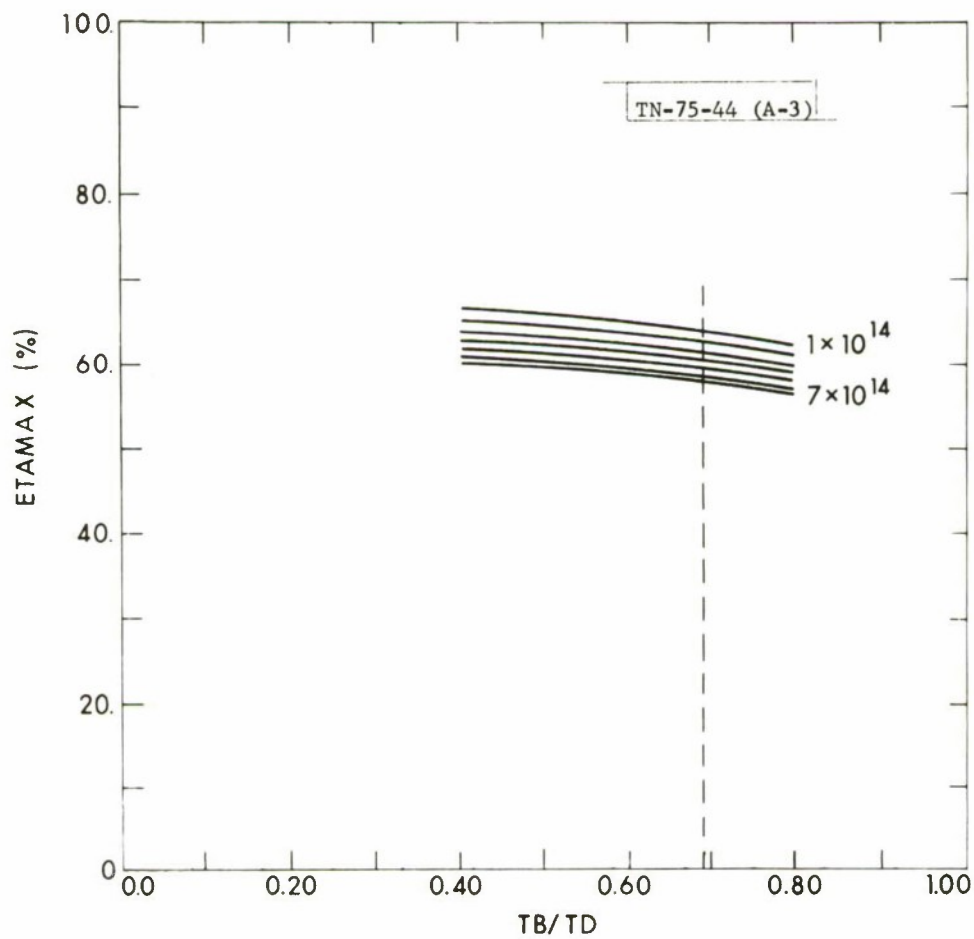
Fig. A-1. Output power density versus τ_b/τ_d.

Fig. A-2. Minimum efficiency versus τ_b/τ_d.

69

Fig. A-3. Maximum efficiency versus τ_b/τ_d.

10^6

10^5

10^4

10^3

10^2

PODN (W/C **2)

TN-75-44 (A-4)

12

5

0.0   0.20   0.40   0.60   0.80   1.00

TB / TD
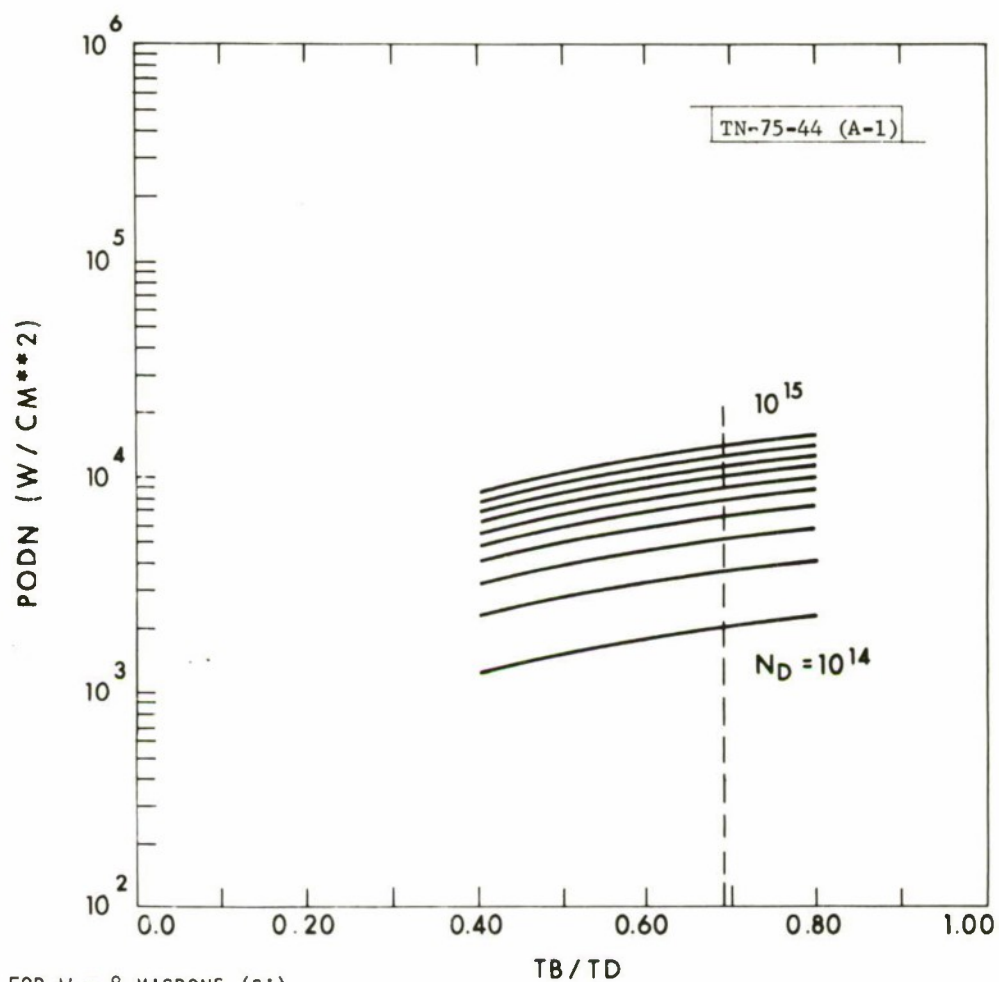
FOR N_d = 5 × 10^{14}/cm^3 (Si)
W IN MICRONS IS THE CONSTANT PARAMETER

Fig. A-4. Output power density versus τ_b/τ_d.

71

Fig. A-5. Maximum efficiency versus τ_b/τ_d.

Fig. A-6a.   Minimum efficiency versus τ_b/τ_d.
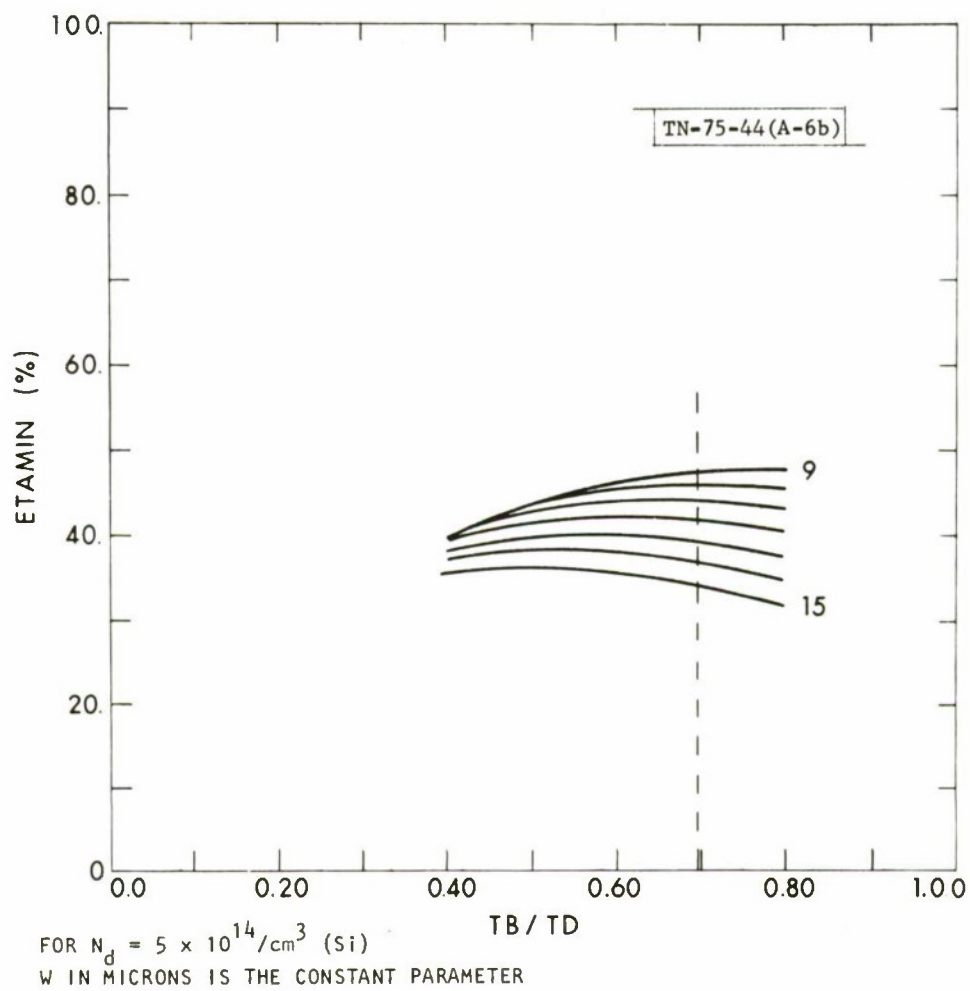
Fig. A-6b. Minimum efficiency versus τ_b/τ_d.

74

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This report presents a comprehensive design criteria for EBS RF power amplifiers which incorporates all pertinent design parameters associated with both the electron beam and semiconductor diode targets. The derivation of the design model is described in detail, and an example amplifier design is carried out yielding an optimum set of device specifications and summary of predicted performance.

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